PLD Design Flow: GAL, Verilog

Summary

This document describes the step-by-step process to create, simulate, and implement a digital design on a GAL PLD using the Cadence/Orcad design suite for simulation and the ispLEVER tools for implementation.

Required Software

- Lattice ispLEVER version 2.0
- Cadence NC-Simulator
- Xeltek SUPERPRO 280 universal programmer software, version 3.0

Required Hardware

- GAL22V10 generic array logic device
- Xeltek SUPERPRO 280 universal programmer
- floppy disk

Boldface type indicates comments that are particularly critical to the success of your project and/or prevents the destruction of your device.

What to Do:	How To Do It:
Create a Conceptual Design	
Draw I/O block diagram of your circuit (i.e. rectangle with pins sticking out and a name for each pin/signal)	Use a piece of paper and pen or pencil to do this! You may need to clarify some details using a manner that the design can easily be changed before jumping in with the computer tools.
Draw a diagram of your circuit components and their interconnections	See above. The diagram will help you visualize the hardware before writing the HDL.
Enter Your Design:	
Set up design directory	Create a new folder for your design files.
Run the Cadence NC-Simulator software	Run Programs | Cadence Design Systems | Affirma Design and Verification | NCLaunch

What to Do:	How To Do It:
Change your working directory	File | Set Design Directory Change the design directory to the folder you created above (only the first time your run the program) create a cds.lib file
Create a new Verilog file for the circuit description	Select "File | EditNewFile" If you are not already there, navigate to where you want the file to be saved and enter a file name (use the .v extension). Click on the "Save" button. This will bring up notepad. Begin writing your Verilog code. (possible bug depending on your set-up: if you click OK on the pop-up window, and notepad closes, reopen the file by selecting the file in the directory window and clicking on the "Browsers | Edit the currently selected file" button on the Toolbar.)
Enter your Verilog circuit description	Enter text as needed. Save your file (use Ctrl-S or push the save-to-disk icon). <u>Example Verilog circuit description:</u> *module Demo (a,b,c);* *input a;* *output b;* *output [2:0] c;* *assign b = ~a;* *assign c = {a,a,a};* *endmodule*

What to Do:	How To Do It:
Compile the circuit description to check for syntax errors.	Select the file under the working directory (in the left-hand side of the window). Click on the “Tools | Launch **Verilog** Complier” button on the Toolbar. The compiled circuit should appear under the “worklib” directory in the right-hand side of the window. You may need to expand the “worklib” directory to see it. If it does not appear, refresh the screen. Error messages will show up in red in the “nclaunch>” field at the bottom of the window. **All errors MUST be corrected before proceeding.**
Verify Your Design Using Simulation	
Write a testbench file instantiating your Design	Create a testbench file (Select “File | EditNewFile” then reopen using the “Browsers | Edit the currently selected file” button on the Toolbar.). Write the testbench file and save. Compile the testbench file to check for syntax errors (“Tools | Launch **Verilog** Complier” button on the Toolbar.)
Elaborate the circuit description to turn the Verilog description into a netlist that can be simulated.	Expand the “worklib” directory on the right-hand side of the window. Select the testbench filename, and the “Tools | Launch Elaborator” button on the Toolbar should activate. Click on the “Tools | Launch Elaborator” button on the Toolbar. Error messages will show up in red in the “nclaunch>” field at the bottom of the window. **All errors MUST be corrected before proceeding.**

What to Do:	How To Do It:
Simulate your design	Open the “Snapshots” directory on the right-hand side of the window. Select the testbench file and the “Tools | Launch Simulator” button on the Toolbar should activate. Press the “Tools | Launch Simulator” button and the simulator window should appear. Press the “Play” button to run the simulation. Binary results will be shown in the text field at the bottom of the window.

What to Do:	How To Do It:
View waveforms of your simulation.	Note: You must have the two following lines in your testbench in order to obtain waveforms: *$shm_open("waves.shm");* *$shm_probe("AC");* To view waveforms, choose the waveforms that you want to diplay from the testbench file displayed at the top of the window. Multiple signals can be selected by holding the ctrl key down. The waveforms will appear in the order that you select them. Click on the “Waveform View” button on the tool bar. This will bring up the waveform viewer. All of your signal names should appear. If you have already run your simulation, to get the waveforms to appear, you must rerun your simulation. Go to “File | Reset Simulation” to rerun the simulation. The waveforms should appear. Alternatively, click on the “Tools | Display waveforms” button on the toolbar in the simulator window (waveforms icon). A waveforms window will appear. Select “Windows | NewDesignBrowser”. A new window will appear. Select the testbench file. All of the inputs, outputs, and internal nodes/variables will appear in the right-hand side of the window. Select the signal that you want to observe. Multiple signals can be selected by holding the ctrl key down. The waveforms will appear in the order that you select them. Press the waveform icon on the Tool Bar. The waveforms should appear in the waveform window. Signals may be removed or grouped into busses by right clicking on the signal name.

What to Do:	How To Do It:
Iterate until your design is correct	If the simulation is not correct, you must go back to your .v file and modify to correct the behavioral problem. If you change your source file, select “File | Reinvoke Simulation” to resimulate using your new file. You may resimulate an unchanged file by selecting “File | Reset Simulation”. You may single step through a simulation by using the small “Play” buttons. This sometimes help you in debugging your circuit description. Leave all of your windows open! If you resimulate, your windows will automatically update.
Do NOT proceed until your design simulates correctly according to your design specs!!	
Convert Your Design Files to Produce a JEDEC File:	
Start ispLEVER	In Windows, do Start | Programs | Lattice Semiconductor | ispLEVER
Start a new project in ispLEVER	Select “File | New Project” Enter a name for your project. It is recommended that you also create a new folder for your project, since the software will generate many files for your single project. Do not use any special characters in your project name or folder name. In particular, do not use spaces. Select “Schematic/Verilog HDL” for your project type. Confirm that you have no spaces in your project name or folder by looking at the top blue strip of the Project Navigator window.

What to Do:	How To Do It:
Specify the device type	Right click on the yellow and black device icon in the left panel and choose “Select New Device”. Select “GAL Device” for Family. Select “GAL22V10B” for Device. Select “24PDIP” for package. Select “-15” for speed grade. Click “OK” and say “Yes” to prompt about changing device kits, and say “Yes” to prompt about losing previous constraints.
Add your Verilog description to the project	Right click on the yellow and black icon and choose “Import”. Choose the .v file that you have simulated (NOT the testbench file - it will not synthesize!)
Create a JEDEC file	Single click the yellow and black device icon in the left panel. Double click the “JEDEC File” in the right-hand side panel.
Confirm your inputs and outputs were connected to the correct pins	Double click “Chip Report” Review the pinout diagram to confirm that it is correct. Note: Do not be concerned if you see some of your outputs indicated as complemented (for example, your output signal is called “Dout” and it appears in the chip report as “!Dout”.) This is merely an indication of the specific method used to create the Boolean expression for that output. The chip output levels will behave as they did in simulation.
Always confirm that the input and output pins have been placed correctly BEFORE placing the GAL in your circuit!!	

What to Do:	How To Do It:
Locate your JEDEC file	Open Windows Explorer window (hold down Windows key and press E) Navigate to your project folder. Note that the path to your project is contained in the title bar of the Project Manager window. Alternatively, do “File | Full Project Path”. Locate the .JED file.
Program GAL with JEDEC File:	
Move your file to the machine tied to the burner	Copy your .JED file to a floppy disk. Take your floppy disk to the computer at the front of the room.
Start Xeltek programmer application	Double click onthe SP280 icon.
Select GAL device	Select “Device | Select” Choose “PLD” option on the right side of the panel. Select “Lattice” for Manufacturer. Select “GAL22V10” for Device name.
Load JEDEC file	Select “File | Load” Navigate to your .JED file and select it.
Insert GAL in device programmer	**Always carry your GAL chip in a piece of conductive foam to avoid causing damage from electrostatic discharge (ESD).** **Notched end of the chip is oriented upwards (see the drawing on the left side of the programmer). If device does not have a notch, then ensure that pin 1 (marked by a dot) is at the upper left.** **Non-notched end of chip is placed flush at bottom of the socket.** Close the lever at the lower right corner of the socket to properly connect the chip to the socket.

What to Do:	How To Do It:
Program the GAL	Select “Device | Run” Select “Program” for Function Click “Run” button to program the GAL
Take your GAL back to your test set-up	**Place your GAL back into the conductive foam before moving the chip to your test set-up!!!!**
Test Your Design	
Apply external stimulus from your own circuitry	The GAL is a 5V device. **Ensure that any waveforms you apply to the circuit swing from 0 to 5 volts BEFORE applying them to your circuit. Otherwise, you may destroy the device!**