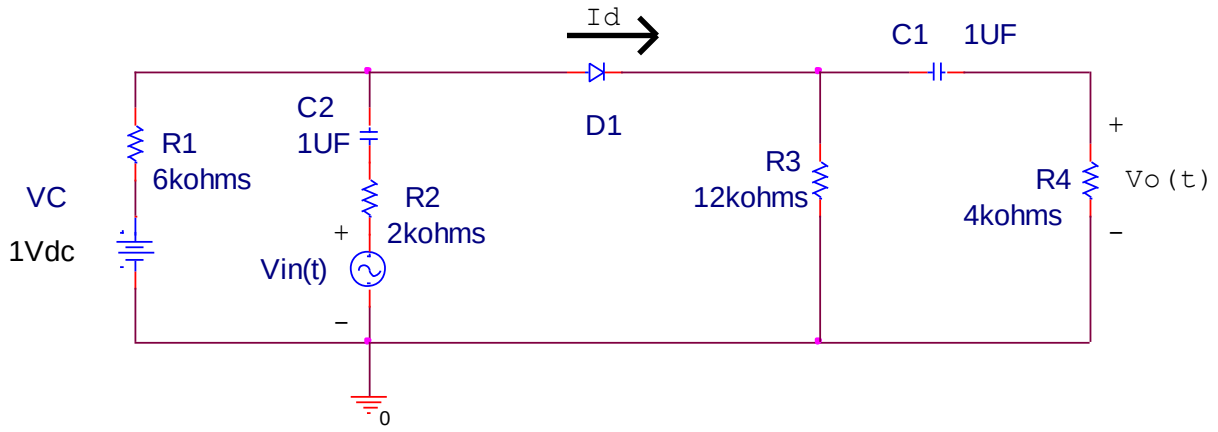
ECE250-2 Final Exam (165 Points, Maximum)
Spring Quarter, May 25, 2010
Open Laptop Maple, 3 Pre-published Equation Sheets Attached, Closed book and notes

Name: _____ **CM#**_____

The first part of this exam (Problem 1 – 8) is objective (multiple choice and fill-in-the-blank). You need ***not*** show your work. You must circle ***one answer only*** on each multiple choice question. ***1.5 points per answer***.

1) (10.5 points) In the audio signal switching circuit below, assume that the diode has ***n = 1.5*** and reverse saturation current ***Is = 0.3 nA***, and that capacitor C1 is a short circuit at the frequency of vin(t). Assume room temperature, with a thermal voltage of $V_T = 25.7$ ***mV***.



a) Using the ideal diode equation (***not*** the simpler 0.7 V piecewise linear model), find the ***dc component*** of the diode current "Id" when the dc control voltage VC = 1 V. Note that there are TWO capacitors in this circuit: C1 and C2.

(a) 30.83 μA (b) 47.92 μA (c) 52.33 μA (d) 78.92 μA (e) 101.28 μA

b) Find the ac small-signal resistance of the diode "rd" when VC = 1 V.
(a) 385.07 Ω (b) 745.3 Ω (c) 494.1 Ω (d) 813.8 Ω (e) 1250 Ω

c) Find the ac gain Av = vo/vin when the dc control voltage VC = 1 V. Assume capacitors C1 and C2 exhibit negligible impedance at the signal frequency.
(a) 0 (b) 0.137 (c) 0.391 (d) 0.472 (e) 0.678 (f) 0.750

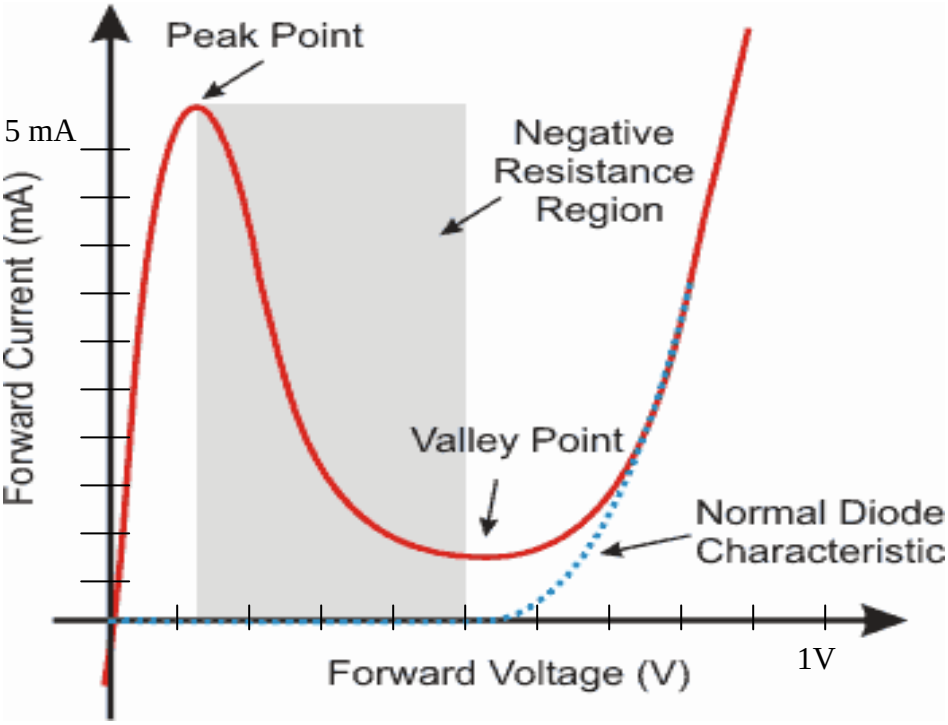
d) Find the ac gain Av = vo/vin when the dc control voltage VC = 0 V.
(a) 0 (b) 0.137 (c) 0.391 (d) 0.472 (e) 0.678 (f) 0.750

e) Find the magnitude of the steady-state dc voltage across capacitor C1 when the control voltage VC = 1 V.
(a) 0 V (b) 0.137 V (c) 0.259 V (d) 0.370 V (e) 0.539 V (f) 0.652 V (g) 0.75 V

f) In ORCAD PSPICE, a resistor is assigned a value of "10M". The value of this resistor is
(a) 10 x 10^{-3} ohms (b) 10 ohms (the "M" does not matter) (c) 10 x 10^{6} ohms.

g) In a ORCAD PSPICE simulation schematic diagram, which of the following is *NOT* a valid way of specifying the value of a 1 kΩ resistor:
(a) 1000 (b) 1k (c) 1kOhm (d) 1000ohms (e) 1k Ohm

2) *(9 pts) Tunnel diodes* exploit a strange quantum phenomenon called *resonant tunneling* to provide interesting forward-bias characteristics. When a small forward-bias voltage is applied across a tunnel diode, it begins to conduct current. As the voltage is increased, the current increases and reaches a peak value called the *peak current* (I_P). If the voltage is increased a little more, the current actually begins to *decrease* until it reaches a low point called the *valley current* (I_V). If the voltage is increased further yet, the current begins to increase again, this time without decreasing into another "valley." The current/voltage plot for a typical tunnel diode is shown in the following illustration:



Find three possible solutions for diode voltage and current (within reasonable limits of graphical accuracy) if this tunnel diode is forward biased by connecting it ***in series*** with a 1.0 V dc source and a 200 ohm resistor.

Solution 1: Vd = _____ Id = _____

Solution 2: Vd = _____ Id = _____

Solution 3: Vd = _____ Id = _____

3) (13.5 pts) A ***full-wave*** diode bridge rectifier is made from four identical diodes, each modeled with a forward voltage drop $V\gamma = 0.7$ V; a capacitor; and a 120 Vrms, 60 Hz step-down ac transformer. The circuit must deliver 25 Vdc across a 50-ohm load with less than 0.25 V peak-to-peak ripple. Assume the power source is to be connected to a standard 120Vrms, 60 Hz power line.

   a) What should the ***RMS*** voltage (***not the peak voltage or peak-to-peak voltage***) be at the secondary winding (output) of the ac transformer?
   (a) 12.4 Vrms (b) 14.6 Vrms (c) 18.8 Vrms (d) 20.0 Vrms (e) 20.7 Vrms (f) 26.5 Vrms

   b) What is the approximate minimum acceptable value of the capacitor?
   (a) 8.3 mF (b) 6.4 mF (c) 4.1 mF (d) 2.5 mF (e) 16.7 mF (f) 200 mF

   c) What is the approximate average (dc) load current that flows through the 50 ohm load?
   (a) 100 mA (b) 200 mA (c) 300 mA (d) 400 mA (e) 500 mA (f) 0

   d) What is the approximate average (dc) current that flows through any one of the four diodes?
   (a) 100 mA (b) 200 mA (c) 250 mA (d) 400 mA (e) 500 mA (f) 0

   e) What minimum peak inverse voltage (PIV), or peak reverse-bias voltage, must be withstood by any one of the diodes? (Circle the closest answer.)
   (a) 12.5 V (b) 25 V (c) 25.8 V (d) 26.4 V (e) 1.4 V (f) 50 V (g) 51.4 V (h) 0 V

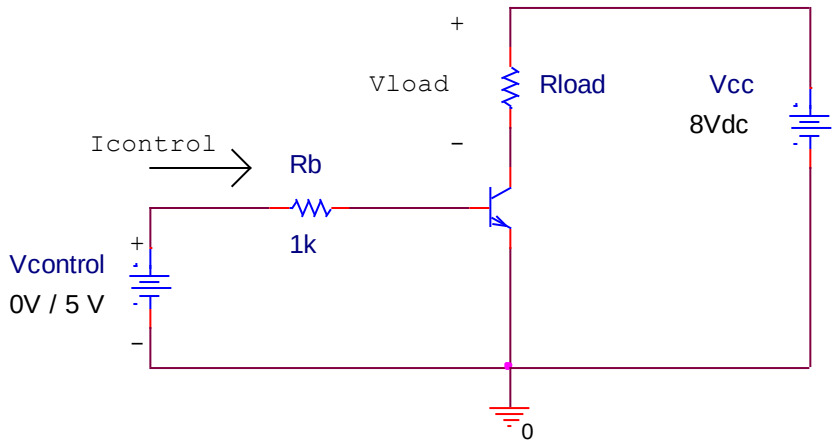
   f) What is the frequency of the ripple voltage?
   (a) 0 Hz (b) 60 Hz (c) 120 Hz

   g) If the 4-diode full-wave bridge rectifier in the design above is replaced by a single-diode, half-wave rectifier that still delivers about 25.0 Vdc across the 50 ohm load resistor, the capacitor value must be approximately _?_ to obtain approximately the same ripple voltage at the output.
   (a) doubled (b) halved (c) quartered (d) left the same

   h) For the half-wave rectifier of Part G, what is the frequency of the ripple voltage?
   (a) 0 Hz (b) 60 Hz (c) 120 Hz

   i) For the half-wave rectifier of Part G, the average current through the diode (compared to the average current through any one of the diodes in the original full-wave diode bridge rectifier circuit) is approximately
   (a) doubled (b) halved (c) quartered (d) left the same

4) (10.5 pts) An NPN BJT with a ***β = 75***, ***Vcesat = 0.1 V***, ***Vbeon = 0.70 V*** is used to switch a high current, 8-volt load, modeled by load resistor "R_{load}", on and off using a relatively low-current 0V / 5V controlling source such as a digital logic signal generated by a microcontroller. (Note that even though we are modeling the load as the resistor R_{load}, it might actually be a high power device like a light bulb, a motor, or a heating element.)



a) How small can the load resistor (Rload) be, and still be switched fully on (V_{load} = 7.9 V) and off (V_{load} = 0V) by this circuit, assuming that the control voltage Vcontrol switches between 5 V (load on) and 0 V (load off)?
(a) 24.5 Ω (b)33.5 Ω (c) 73.8 Ω (d) 89.7 Ω (e) 138.4 Ω

b) What current must the control voltage source "Vcontrol" be capable of sourcing when Vc = 5 V?
(a) 2.15 mA (b) 3.15 mA (c) 4.3 mA (d) 5.15 mA (e) 0

c) If RL = 50 ohms and Vcontrol = 0 V, how much power is consumed in (delivered to) RL?
(a) 0 W (b) 15.8 mW (c) 0.305 W (d) 0.475 W (d) 0.708 W (e) 1.25 W

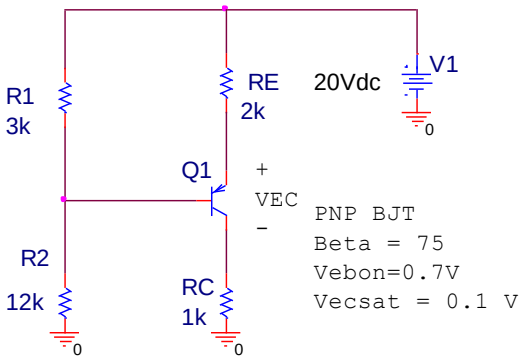
d) If RL = 50 ohms and Vcontrol = 5 V, how much power is consumed in (delivered to) RL?
(a) 0 W (b) 15.8 mW (c) 0.305 W (d) 0.475 W (d) 0.708 W (e) 1.25 W

e) If RL = 50 ohms, and if Vcontrol = 5 V, how much power is dissipated as heat in Q1? (You may ignore the base current in this calculation, that is, assume P_{BJT} = Vce*Ic.)
(a) 0 W (b) 15.8 mW (c) 0.305 W (d) 0.475 W (d) 0.708 W (e) 1.25 W

f) If RL = 50 ohms and Vcontrol = 2 V (this represents an undesirable condition, where the controlling source Vc has ***not*** delivered a high enough voltage to drive the BJT into saturation), how much power is delivered to the load resistor, RL?
(a) 0 W (b) 15.8 mW (c) 0.305 W (d) 0.475 W (d) 0.708 W (e) 1.25 W

g) If RL = 50 ohms, and if Vcontrol = 2 V, how much power is dissipated as heat in Q1? (You may ignore the base current in this calculation, that is, assume P_{BJT} = Vce*Ic.) This is obviously an undesirable condition!
(a) 0 W (b) 15.8 mW (c) 0.305 W (d) 0.475 W (d) 0.708 W (e) 1.25 W

5) (6 pts) Consider the PNP BJT circuit below. Assume that β is 75.

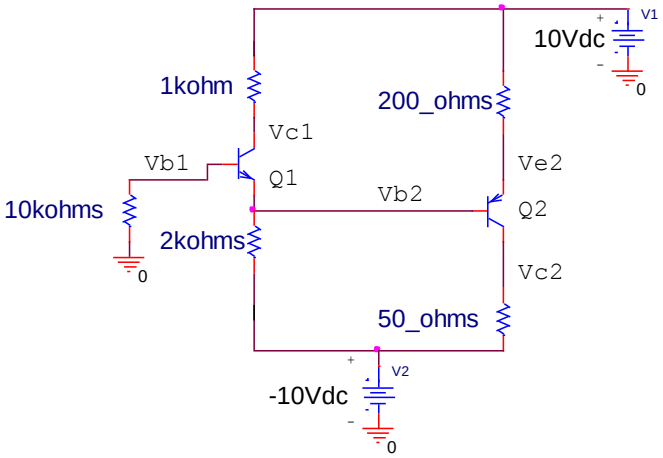


a) V_{EC} = (a) 14.92 V (b) 15.05 V (c) 15.15 V (d) 15.23 V (e) 15.37 V

b) If the PNP BJT's β value is increased from 75 to ***infinity***,
The infinite β assumption implies that __(i)___ and also that ___(ii)____.
(i) (a) Ib = 0 (b) Ic = 0 (c) Ie = 0
(ii) (a) Ib = Ie (b) Ib = Ic (c) Ie = Ic

c) Recalculate V_{EC} assuming that β = infinity.
V_{EC} = (a) 14.92 V (b) 15.05 V (c) 15.15 V (d) 15.23 V (e) 15.37 V

6) (6 pts) Consider the circuit below, where the NPN BJT Q1 has β = ***infinity***, Vbeon = 0.7 V, and Vcesat = 0.1 V. The PNP BJT Q2 has β = ***infinity***, Vebon = 0.7 V, and Vecsat = 0.1 V.



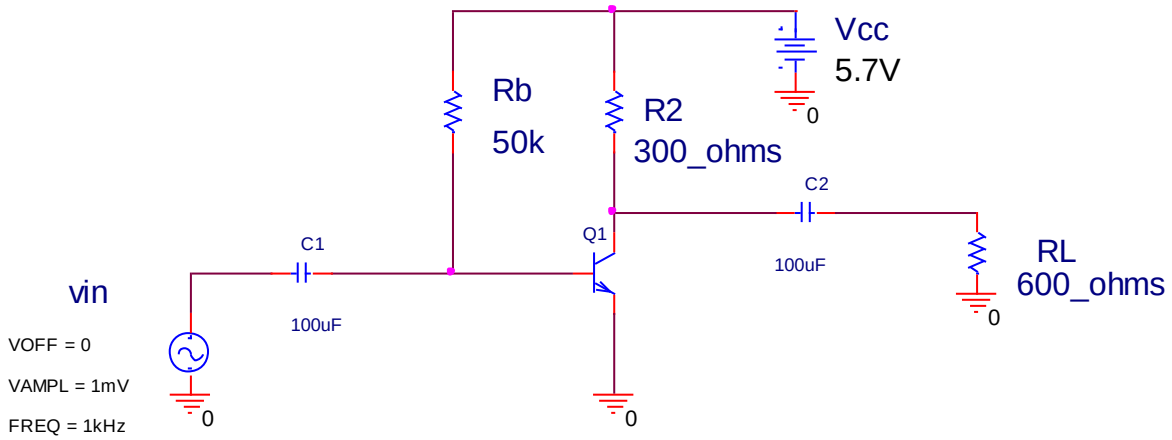
Assuming that both BJTs exhibit ***infinite*** β,
a) Vce1 = (a) 3.83 V (b) 6.05 V (b) 6.92 V (c) 7.5 V (d) 8.80V (e) 12.45 V (f) 18.5 V

b) Vec2 = (a) 3.83 V (b) 6.05 V (b) 6.92 V (c) 7.5 V (d) 8.80V (e) 12.45 V (f) 18.5 V

Now repeat the analysis assuming both BJTs have ***β = 75***, rather than infinite β.
c) Vce1 = (a) 3.83 V (b) 6.05 V (b) 6.92 V (c) 7.5 V (d) 8.80V (e) 12.40 V (f) 18.75 V

d) Vec2 = (a) 3.83 V (b) 6.05 V (b) 6.92 V (c) 7.5 V (d) 8.80V (e) 12.40 V (f) 18.75 V

7) (16.5 points) Given the NPN BJT circuit below where the BJT has the following parameters:
Vbe_{ON} = 0.7 V, **β = 75**, **VA = 50 V**, and **Vce_{SAT} = 0.1 V**, **n = 1**, **V_T = 25.7 mV**



a) Find the Q-point of the BJT: Vceq and Icq. (Ignore VA when performing this DC analysis.)

i) Vceq = (a) 1.36 V (b) 2.95 V (c) 2.72 V (d) 3.45 V (e) 5.69 V

ii) Icq = (a) 3.5 mA (b) 7.5 mA (c) 9.25 mA (d) 12.5 mA (e) 14.25 mA

b) Find the BJT small-signal ac model parameters: r_π and r_o

i) r_π = (a) 255.7 Ω (b) 257 Ω (c) 287 Ω (d) 6.666 kΩ (e) 9.784 kΩ

ii) r_o = (a) 255.7 Ω (b) 257 Ω (c) 287 Ω (d) 6.666 kΩ (e) 9.784 kΩ

c) Find the general voltage amplifier model parameters: Avo, Rin, Rout (RL removed)

i) Avo = (a) 0.875 (b) 0.954 (c) -56.67 (d) -83.78 (e) -127.38

ii) Rin = (a) 255.7 Ω (b) 257 Ω (c) 287 Ω (d) 6.666 kΩ (e) 9.784 kΩ

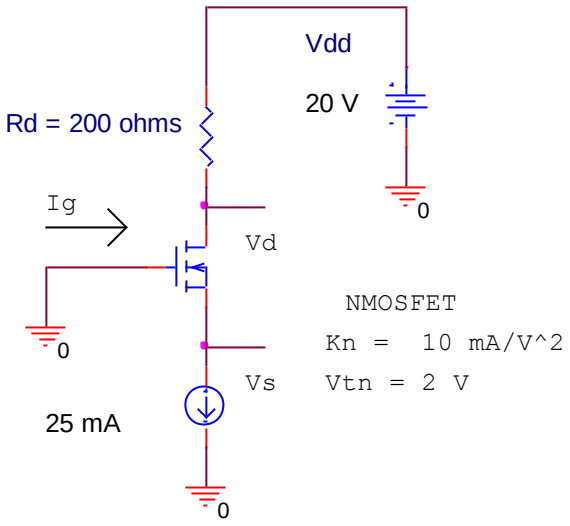
iii) Rout = (a) 255.7 Ω (b) 257 Ω (c) 287 Ω (d) 6.666 kΩ (e) 9.784 kΩ

d) The overall loaded voltage gain Av = (a) 0.875 (b) 0.954 (c) -56.67 (d) -83.78 (e) -127.38

e) With ***RL present***, calculate how far Vce may swing above Vceq and also how far Vce may swing below Vceq. Then find the maximum symmetrical output voltage swing, assuming that for lower distortion, we require that ***Vcemin = 0.5 V*** and also ***Icmin = 0.5 mA***. Remember to include the effects of the Early Voltage, VA in your calculations.

i) Vce may swing _?_ above Vceq (a) 1.36 V (b) 2.95 V (c) 2.72 V (d) 3.45 V (e) 5.7 V
ii) Vce may swing _?_ below Vceq (a) 1.36 V (b) 2.95 V (c) 2.72 V (d) 3.45 V (e) 5.7 V
iii) Maximum (peak-to-peak) symmetrical output voltage swing =
(a) 1.36 Vpp (b) 2.95 Vpp (c) 2.72 Vpp (d) 3.45 Vpp (e) 5.7 Vpp (f) 5.9 Vpp

8) (9 pts) The NMOSFET in the circuit below has conduction parameter Kn = 10 mA/V^2, and a threshold voltage Vtn = 2 V. It is biased with a constant current source of 25 mA.



a) Find the operating mode, drain voltage w.r.t. ground (Vd), and source voltage w.r.t ground (Vs) of the NMOSFET:

i) Operating mode: (a) ohmic (b) saturation (c) cut off

ii) Vd: (a) -3.58 V (b) -5 V (c) -6.636 V (d) -10.0 V (e) -10.89 V (f) 6 V (g) 15 V (h) 10 V

iii) Vs: (a) -3.58 V (b) -5 V (c) -6.636 V (d) -10.0 V (e) -10.89 V (f) 6 V (g) 15 V (h) 10 V

b) Find the operating mode, Vd, and Vs of the NMOSFET if the constant current source in the circuit above is changed from 25 mA to 125 mA.

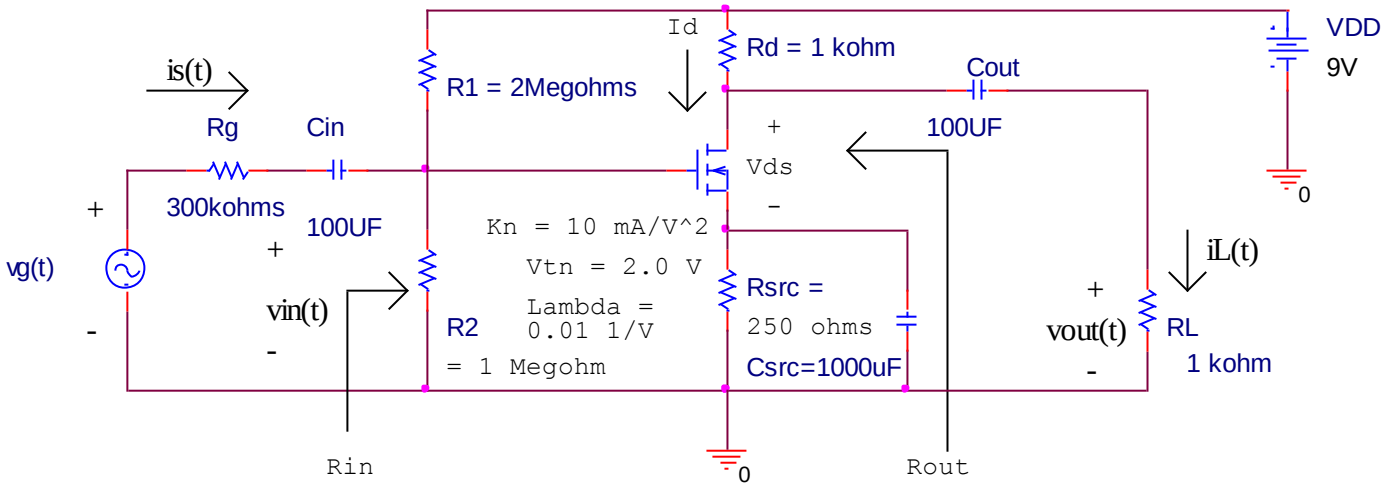
i) Operating mode: (a) ohmic (b) saturation (c) cut off

ii) Vd: (a) -3.58 V (b) -5 V (c) -6.636 V (d) 4.5 V (e) 5.5 V (f) 6 V (g) 15 V (h) 10 V (i) 0 V

iii) Vs: (a) -3.58 V (b) -5 V (c) -6.636 V (d) 4.5 V (e) 5.5 V (f) 6 V (g) 15 V (h) 10 V (i) 0 V

9) (32 points) Common-Source Amplifier (FOR PROBLEMS 9 – 11, PLEASE SHOW YOUR WORK NEATLY AND COMPLETELY IN ORDER TO RECEIVE CREDIT)

Note: The NMOSFET parameters ***K_N = 10 mA/V^2*** and ***V_{TN} = 2.0 V***, and ***λ = 0.01 V^{-1}***.



a) (8 pts) Find the quiescent (dc) values of Vds, Vgs, and Id; assuming the MOSFET is in saturation mode. Then use your results to show that this assumption is correct. (As usual, ignore the effects of channel-length modulation (λ) in your dc calculations.)

Vgsq = _____

Vdsq = _____

Idq = _____

Demonstration that NMOSFET is operating in saturation mode:

_____

b) (2 pts) Calculate the ac small-signal NMOSFET parameters ro and gm from your dc analysis results

gm = _____

ro = _____

c) (8 pts) Assuming that C1, C2, and C3 are all short circuits at the 1 kHz signal frequency, CAREFULLY construct the ac model of the NMOSFET amplifier circuit, and from this ac model, calculate the small-signal open-circuit voltage gain Avo = vout/vin with RL removed, Rin, and Rout.

Small-Signal Model

Avo = _____
Rin = _____
Rout = _____

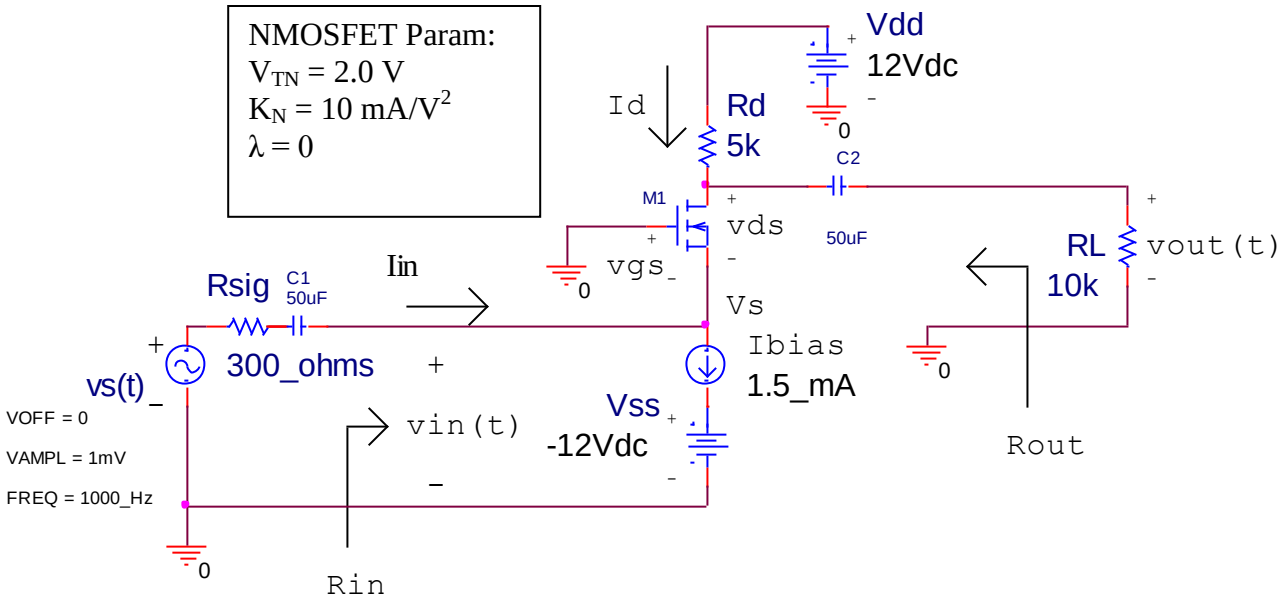
d) (4 pts) Draw the general ac amplifier model in the space below, showing Rin, Rout, and Avo. Also include the source and load terminations. Then calculate the overall voltage gain, transducer voltage gain, and current gain.

Av = vout/vg = _____
Avt = vout/vin = _____
Ai = i_L/i_S = _____

e) (10 pts) Calculate how far Vds can swing above and below the Q-point value, Vdsq. Assume (as we did in class) that Vds is allowed to swing between cutoff (Id = 0) and the start of the ohmic region.

Vds can swing _____ below Vdsq
Vds can swing _____ above Vdsq

10) (32 pts) Consider the "***Common-Gate***" amplifier below:



A. (10 pts) Note that this time the NMOSFET has **λ = 0**. Find the numerical values of Vgs_Q, Id_Q, Vds_Q, Vs_Q. From these results check to ensure the NMOSFET is saturated.

Vgs_Q = _____

Id_Q = _____

Vs_Q = _____

Vds_Q = _____

Check for Saturation:

_____

B. (1 pts) Find the ac small-signal NMOSFET model parameter "gm"

gm = _____

C. (15 pts) Draw the AC small-signal model ***carefully*** in the space below. As usual, assume that the coupling capacitors C1 and C2 act like short circuits at the signal frequency. Then, referring to the AC model drawn above, ***derive literal expressions*** for Avo = vout/vin with RL removed, Rin, and Rout (all three expressions should be in terms of ***gm*** and ***Rd***) in the space below.

Small-Signal AC Model

Derivation of Literal Expressions (in terms of gm and Rd) for Avo, Rin, Rout

D. (2 pts) Find numerical values for Rin, Rout, Avo = vout/vin (with RL removed of course)

Rin = _____

Rout = _____

Avo = _____

E. (2 pts) Draw the general voltage amplifier model, clearly labeling Rin, Rout,and Avo. Also draw the generator and source terminations.

F. (2 pts) Referring to the general voltage amplifier model drawn above, determine Av = vout/vs and Avt = vout/vin

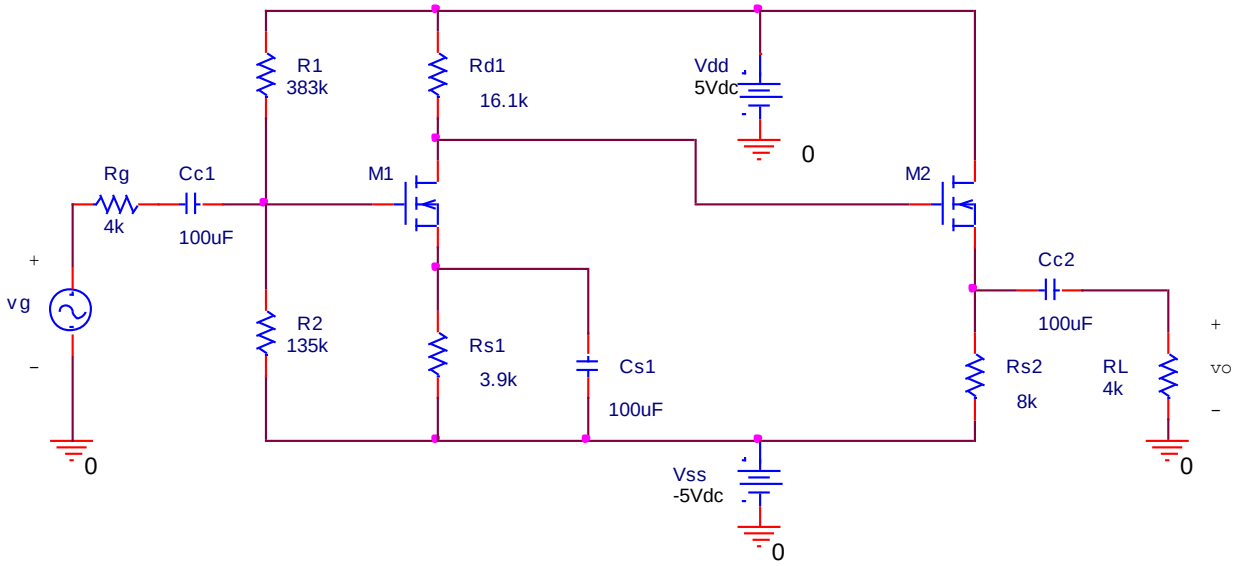
Av = _____
Avt = _____

11) (20 points) ***Small-Signal AC Modelling***

Neatly and completely draw the "small-signal" ac model of this circuit in the space below. Express the ac parameters of the NMOSFETs ***symbolically*** in your ac model (***gm1, ro1, gm2, ro2***). *YOU NEED NOT dc analyze the circuit first to determine the numerical values of these ac model parameters*.

Be sure to label **vg, Rg, R1, R2, Rd1, Rs2, RL and vo** in your model. You may ***ignore*** the numerical values of the components that are specified. Also be sure to :

(1) Label the terminals of NMOSFET "M1" (**G1, D1, S1**) and of M2 (**G2, D2, S2**)
(2) Label the strength of each dependent current source (expressions involving gm1, gm2, etc.)
(3) Label and show the polarities of the control voltages (**vgs1, vgs2**) for each dependent current source.



ECE250 Equation Sheet Test 1 April 1, 2010 (KEH)

Diode Equation: $Id = Is \cdot (e^{Vd/(nV_T)} - 1)$ where Is = reverse saturation current. Is ***DOUBLES*** for every 10 degree C rise

Vd is the anode-to-cathode voltage and Id is current flowing into anode

Thermal Voltage: $V_T = kT/q = 25.7$ mV at room temperature T = 300K.

DC load voltage: $Vdc = V_{m,s} - 0.7V - V_r/2$ (half-wave rect) $Vdc = = V_{m,s} - 1.4V - V_r/2$ (full-wave rect)

Half-wave rectifier ripple voltage: $V_r = \dfrac{(V_{m,s} - 0.7V - V_r/2)/R_L}{f_{source} \cdot C}$ $V_{m,s}$ = peak source voltage

Full-wave diode bridge rectifier ripple voltage: $V_r = \dfrac{(V_{m,s} - 1.4V - V_r/2)/R_L}{2 f_{source} \cdot C}$ $V_{m,s}$ = peak source voltage

Full-wave diode bridge peak diode current: $I_{d\max} = \dfrac{V_m}{R_L} \cdot (1 + 2\pi) \cdot \sqrt{\dfrac{V_m}{2 \cdot V_r}}$, where $V_m = V_{m,s} - 2(0.7V)$

Small-Signal ac Model of Diode: $rd = \dfrac{n \cdot V_T}{Id_Q}$, where Id_Q is the dc (quiescent) component of the diode current.

Plotting Load Lines over nonlinear element's IV curve: First find Thevenin equivalent "looking out" from the terminals of the nonlinear element. Then plot load line: $I_{INTERCEPT}$ = Vth/Rth, and $V_{INTERCEPT}$ = Vth

Multiple Diode Analysis using 0.7 V battery model of diode: Define Id's flowing into each anode. Define Vd's anode-to-cathode. Guess which diodes are ON and replace them with 0.7 battery, replace OFF diodes with open circuit. Analyze circuit. Check to ensure diodes that are assumed ON have Id > 0, and diodes that are assumed OFF have Vd < 0.7 V.

Carrier Concentration in Intrinsic Si (1/cm^3): $n_i^2 = BT^3 e^{-Eg/kT}$

at T=300K: B=5.4x10^{31}/(K^{3}cm^6), Eg=1.12 eV, k= Boltzmann's Constant = 8.62x10^{-5} eV/K, n_i=1.5 x 10^{10} 1/cm^3

Diffusion Current Density (A/cm^2): $J_p = -qD_p \dfrac{dp}{dx}$ $J_n = qD_n \dfrac{dn}{dx}$ q = 1.6 x 10^{-19} Coulombs

D_p = 12 cm^2/s, D_n = 34 cm^2/s

Drift current Density (A/cm^2): $J_{drift} = q(p\mu_p + n\mu_n)E$

Resistivity (Ω-cm) and Resistance (Ω): $\rho = 1/[q(p\mu_p + n\mu_n)]]$ R = ρL/A

Carrier Concentration in n-type Si (1/cm^3): $n_{n0} = N_D$ $p_{n0} = n_i^2/N_D$ ***in p-type Si (1/cm^3)***: $p_{p0} = N_A$ $n_{p0} = n_i^2/N_A$

Built-In Junction Voltage (V): $Vo = V_T \ln(\dfrac{N_A N_D}{n_i^2})$

Depletion Region Capacitance (F): $C_j = \dfrac{C_{j0}}{(1 + \dfrac{V_R}{Vo})^m}$ ***where*** $C_{j0} = \varepsilon_{Si} A/(W_{depletion\_region})_{V_R=0}$

and m = junction grading coefficient = 1/3 to ½,

also note V_R is diode's CATHODE to ANODE voltage = -Vd

ECE250 (KEH) BJT Formula Sheet (For Test 2)

BJT Modes of Operation:

Cutoff	BE junction off, BC junction off
Forward Active	BE junction on, BC junction off
Reverse Active	BE junction off, BC junction on
Saturation	BE junction on, BC junction on

For NPN BJT: Ie referenced flowing OUT of BJT, Ib and Ic both referenced flowing INTO BJT

Vbe_{ON} = 0.7 V, Vce_{SAT} = 0.1 V

For PNP BJT: Ie referenced flowing INTO BJT, Ib and Ic both referenced flowing OUT OF BJT

Veb_{ON} = 0.7 V, Vec_{SAT} = 0.1 V

For forward active NPN and PNP BJTs:

$Ie = Ib + Ic \qquad \alpha = \frac{Ic}{Ie} \quad (0 < \alpha < 1') \qquad \beta = \frac{Ic}{Ib} = \frac{\alpha}{1-\alpha}$

$r_\pi = \frac{n \cdot V_T}{Ib_Q} \qquad ro = \frac{V_A}{Ic_Q} \qquad g_m = \frac{i_c(t)}{v_{be}(t)} = \frac{\beta}{r_\pi}$

DC Q Point Stability Design Rules of Thumb: $(1+\beta)Re = 10R_{TH}$ and $V_{Re} = 1$ V

General Voltage Amplifier AC Model: $Avo = \left(\frac{v_{out}(t)}{v_{in}(t)}\right)$ $R_{in} = \frac{v_{in}(t)}{i_{in}(t)}$ $R_{out} = \left(\frac{v_{test}}{i_{test}}\right)$ ***vin(t) -> 0*** ***RL = infinity***

For CE Amplifier: (*Note, you must know how to derive these, if asked on the test)*

$$Avo = \frac{-\beta \cdot \frac{Rc \cdot ro}{Rc + ro}}{r_\pi + (\beta + 1) \cdot Re_1} \qquad R_{in} = \frac{1}{\frac{1}{R1} + \frac{1}{R2} + \frac{1}{r_\pi + (\beta + 1) \cdot Re_1}} \qquad R_{out} = \frac{Rc \cdot ro}{Rc + ro}$$

DC Load Line: Ic intercept = (Vcc-Vee)/(Rc+Re) Vce intercept = Vcc-Vee Slope = -1/(Rc+Re)

Note: Vee = 0 in a single-ended dc power supply

AC Load Line Slope = -1/([Rc // ro // R_L] + Re1) ***Note: Re1 is unbypassed portion of Re***

For CC (Emitter Follower) Amplifier: (Note, you must know how to derive these, if asked on the test)

$$Av_o = \frac{(\beta + 1) \cdot \left(\frac{Re \cdot ro}{Re + ro}\right)}{r_\pi + (\beta + 1) \cdot \left(\frac{Re \cdot ro}{Re + ro}\right)} \qquad Rbin = r_\pi + (\beta + 1) \cdot \frac{1}{\frac{1}{Re} + \frac{1}{ro} + \frac{1}{R_L}} \qquad R_{in} = \frac{1}{\frac{1}{Rbin} + \frac{1}{R_1} + \frac{1}{R_2}}$$

Rout = (Re // ro) // (r_π + R_1 // R_2 // Rs) / (β + 1) ***NOTE: For "Rin_no_R_L", leave R_L out of the Rbin formula.***

AC Load Line Slope = -1/(Re // ro // RL)

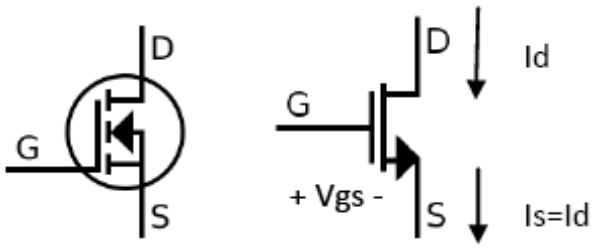
General Voltage Amplifier Model Voltage, Current, Power Gains:

Av = vout/vs = Rin / (Rs + Rin)*Avo*R_L / (Rout + R_L) ***Note: For"Av" of CC Amp, replace Rin by Rin_no_RL***

$$Ai = \frac{i_{out}}{i_{in}} = \frac{\left(\frac{v_{out}}{R_L}\right)}{\left(\frac{v_s}{Rs + Rin}\right)} = Av \cdot \frac{Rs + Rin}{R_L} \qquad Ap = \frac{p_{out}}{p_{in}} = \frac{v_{out} \cdot i_{out}}{v_s \cdot i_{in}} = Av \cdot Ai$$

ECE250 NMOSFET Equation Sheet (For Final Exam)

NMOSFET Sym



Ohmic Mode $Vgs - Vds > V_{TN}$ $Id = K_N \cdot \left[2 \cdot \left(Vgs - V_{TN}\right) \cdot Vds - Vds^2\right]$

Saturation Mode: $Vgs - Vds < V_{TN}$ $Id = K_N \cdot \left(Vgs - V_{TN}\right)^2$

Conduction Parameter: $K_N = k_N \cdot \frac{W}{2 \cdot L}$ Where **k_N = process gain:** $k_N = \frac{\mu_n \cdot \varepsilon_0 \cdot \varepsilon_{ox}}{t_{ox}}$

W = Channel_Width L = Channel_Length μ_n = Surface_Mobility_of_Electrons_in_Silicon

$\varepsilon_0 = 8.854 \cdot 10^{-12} \cdot \frac{F}{m}$ $\varepsilon_{ox} = 3.9$ t_{ox} = Gate_Oxide_Thickness

Small Signal AC Model of NMOSFET:

$$g_m = \left[\frac{d \cdot \left[K_N \cdot \left(Vgs - V_{TN}\right)^2\right]}{dVgs}\right]_{Q\text{-Pt}} = 2 \cdot K_N \cdot \left(Vgs_Q - V_{TN}\right) \qquad r_o = \frac{1}{\lambda \cdot Id_Q} = \frac{V_M}{Id_Q}$$