ECE250 Equation Sheet Test 1 April 1, 2010 (KEH)

Diode Equation: $Id = Is \cdot (e^{Vd/(nV_T)} - 1)$ where Is = reverse saturation current. Is ***DOUBLES*** for every 10 degree C rise

Vd is the anode-to-cathode voltage and Id is current flowing into anode

Thermal Voltage: $V_T = kT/q = 25.7$ mV at room temperature T = 300K.

DC load voltage: $Vdc = V_{m,s} - 0.7V - V_r/2$ (half-wave rect) $Vdc = = V_{m,s} - 1.4V - V_r/2$ (full-wave rect)

Half-wave rectifier ripple voltage: $V_r = \dfrac{(V_{m,s} - 0.7V - V_r/2)/R_L}{f_{source} \cdot C}$ $V_{m,s}$ = peak source voltage

Full-wave diode bridge rectifier ripple voltage: $V_r = \dfrac{(V_{m,s} - 1.4V - V_r/2)/R_L}{2 f_{source} \cdot C}$ $V_{m,s}$ = peak source voltage

Full-wave diode bridge peak diode current: $I_{d\max} = \dfrac{V_m}{R_L} \cdot (1 + 2\pi) \cdot \sqrt{\dfrac{V_m}{2 \cdot V_r}}$, where $V_m = V_{m,s} - 2(0.7V)$

Small-Signal ac Model of Diode: $rd = \dfrac{n \cdot V_T}{Id_Q}$, where Id_Q is the dc (quiescent) component of the diode current.

Plotting Load Lines over nonlinear element's IV curve: First find Thevenin equivalent "looking out" from the terminals of the nonlinear element. Then plot load line: $I_{INTERCEPT}$ = Vth/Rth, and $V_{INTERCEPT}$ = Vth

Multiple Diode Analysis using 0.7 V battery model of diode: Define Id's flowing into each anode. Define Vd's anode-to-cathode. Guess which diodes are ON and replace them with 0.7 battery, replace OFF diodes with open circuit. Analyze circuit. Check to ensure diodes that are assumed ON have Id > 0, and diodes that are assumed OFF have Vd < 0.7 V.

Carrier Concentration in Intrinsic Si (1/cm^3): $n_i^2 = BT^3 e^{-Eg/kT}$

at T=300K: B=5.4x10^{31}/(K^{3}cm^6), Eg=1.12 eV, k= Boltzmann's Constant = 8.62x10^{-5} eV/K, n_i=1.5 x 10^{10} 1/cm^3

Diffusion Current Density (A/cm^2): $J_p = -qD_p \dfrac{dp}{dx}$ $J_n = qD_n \dfrac{dn}{dx}$ q = 1.6 x 10^{-19} Coulombs

D_p = 12 cm^2/s, D_n = 34 cm^2/s

Drift current Density (A/cm^2): $J_{drift} = q(p\mu_p + n\mu_n)E$

Resistivity (Ω-cm) and Resistance (Ω): $\rho = 1/[q(p\mu_p + n\mu_n)]]$ R = ρL/A

Carrier Concentration in n-type Si (1/cm^3): $n_{n0} = N_D$ $p_{n0} = n_i^2/N_D$ ***in p-type Si (1/cm^3)***: $p_{p0} = N_A$ $n_{p0} = n_i^2/N_A$

Built-In Junction Voltage (V): $Vo = V_T \ln(\dfrac{N_A N_D}{n_i^2})$

Depletion Region Capacitance (F): $C_j = \dfrac{C_{j0}}{(1 + \dfrac{V_R}{Vo})^m}$ ***where*** $C_{j0} = \varepsilon_{Si} A/(W_{depletion\_region})_{V_R=0}$

and m = junction grading coefficient = 1/3 to ½,

also note V_R is diode's CATHODE to ANODE voltage = -Vd

ECE250 (KEH) BJT Formula Sheet (For Test 2)

BJT Modes of Operation:

Cutoff	BE junction off, BC junction off
Forward Active	BE junction on, BC junction off
Reverse Active	BE junction off, BC junction on
Saturation	BE junction on, BC junction on

For NPN BJT: Ie referenced flowing OUT of BJT, Ib and Ic both referenced flowing INTO BJT

Vbe_{ON} = 0.7 V, Vce_{SAT} = 0.1 V

For PNP BJT: Ie referenced flowing INTO BJT, Ib and Ic both referenced flowing OUT OF BJT

Veb_{ON} = 0.7 V, Vec_{SAT} = 0.1 V

For forward active NPN and PNP BJTs:

$Ie = Ib + Ic \qquad \alpha = \frac{Ic}{Ie} \quad (0 < \alpha < 1') \qquad \beta = \frac{Ic}{Ib} = \frac{\alpha}{1-\alpha}$

$r_\pi = \frac{n \cdot V_T}{Ib_Q} \qquad ro = \frac{V_A}{Ic_Q} \qquad g_m = \frac{i_c(t)}{v_{be}(t)} = \frac{\beta}{r_\pi}$

DC Q Point Stability Design Rules of Thumb: $(1+\beta)Re = 10R_{TH}$ and $V_{Re} = 1$ V

General Voltage Amplifier AC Model: $Avo = \left(\frac{v_{out}(t)}{v_{in}(t)}\right)$ $R_{in} = \frac{v_{in}(t)}{i_{in}(t)}$ $R_{out} = \left(\frac{v_{test}}{i_{test}}\right)$ ***vin(t) -> 0*** ***RL = infinity***

For CE Amplifier: (*Note, you must know how to derive these, if asked on the test)*

$$Avo = \frac{-\beta \cdot \frac{Rc \cdot ro}{Rc + ro}}{r_\pi + (\beta + 1) \cdot Re_1} \qquad R_{in} = \frac{1}{\frac{1}{R1} + \frac{1}{R2} + \frac{1}{r_\pi + (\beta + 1) \cdot Re_1}} \qquad R_{out} = \frac{Rc \cdot ro}{Rc + ro}$$

DC Load Line: Ic intercept = (Vcc-Vee)/(Rc+Re) Vce intercept = Vcc-Vee Slope = -1/(Rc+Re)

Note: Vee = 0 in a single-ended dc power supply

AC Load Line Slope = -1/([Rc // ro // R_L] + Re1) ***Note: Re1 is unbypassed portion of Re***

For CC (Emitter Follower) Amplifier: (Note, you must know how to derive these, if asked on the test)

$$Av_o = \frac{(\beta + 1) \cdot \left(\frac{Re \cdot ro}{Re + ro}\right)}{r_\pi + (\beta + 1) \cdot \left(\frac{Re \cdot ro}{Re + ro}\right)} \qquad Rbin = r_\pi + (\beta + 1) \cdot \frac{1}{\frac{1}{Re} + \frac{1}{ro} + \frac{1}{R_L}} \qquad R_{in} = \frac{1}{\frac{1}{Rbin} + \frac{1}{R_1} + \frac{1}{R_2}}$$

Rout = (Re // ro) // (r_π + R_1 // R_2 // Rs) / (β + 1) ***NOTE: For "Rin_no_R_L", leave R_L out of the Rbin formula.***

AC Load Line Slope = -1/(Re // ro // RL)

General Voltage Amplifier Model Voltage, Current, Power Gains:

Av = vout/vs = Rin / (Rs + Rin)*Avo*R_L / (Rout + R_L) ***Note: For"Av" of CC Amp, replace Rin by Rin_no_RL***

$$Ai = \frac{i_{out}}{i_{in}} = \frac{\left(\frac{v_{out}}{R_L}\right)}{\left(\frac{v_s}{Rs + Rin}\right)} = Av \cdot \frac{Rs + Rin}{R_L} \qquad Ap = \frac{p_{out}}{p_{in}} = \frac{v_{out} \cdot i_{out}}{v_s \cdot i_{in}} = Av \cdot Ai$$