TMS320C67-BASED DESIGN OF A DIGITAL AUDIO POWER AMPLIFIER INTRODUCING NOVEL FEEDBACK STRATEGY

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The fundamental problem of pulse-width modulation (PWM) based open-loop digital Class-D audio power amplifiers is the inherent nonlinearity of the PWM process, which necessitates the application of a precompensating linearization algorithm. Severe technical difficulties arising from the stringent speed requirements of both electronic circuitry, and digital signal processing devices make the implementation of high-fidelity digital power amplifiers even more challenging, despite today's advanced technology.

A versatile simulation model of a digital power amplifier was developed, and the performance of three existing linearization techniques was evaluated. A digital signal processor based laboratory prototype of a digital power amplifier was designed and built, incorporating two of the simulated linearization methods. The laboratory prototype proves the effectiveness of the linearization methods for low-power PWM-signals. The laboratory prototype was also used to identify further problems associated with the open-loop digital Class-D amplifier concept, such as the influence of a non-ideal switching stage. Finally, an alternative pseudo-feedback strategy was suggested, which employs a linear adaptive filter.

0 INTRODUCTION TO CLASS-D POWER AMPLIFICATION

Modern high-fidelity stereo systems commonly consist of digital signal sources, such as compact disc (CD) players, digital audio tape (DAT) recorders, and digital audio broadcast (DAB) receivers. The digitized music signals are pulse-code modulated (PCM) and usually have 12-bit or 16-bit resolution and sampling frequencies of 32kHz (DAB), 44.1kHz (CD), or 48kHz (DAT). Furthermore, a digital preamplifier often serves as a switching center, incorporating volume and sound control, and sometimes even room or loudspeaker equalization. A single stereo digital-to-analog converter (DAC) can be used to feed the selected source signal after digital-to-analog conversion to an analog power amplifier, which drives the speakers of the system. Those power amplifiers usually have an output power in the range from a few watts, for portable equipment, to several hundred watts, for professional use.

The advantages of digital music storage, transmission, and processing are well-known. Digital systems outperform analog ones with respect to fidelity, reliability, and cost efficiency. Hence, it seems to be reasonable to try to replace even the last two elements in the signal chain – the power amplifier and the loudspeaker – by digital systems. There is no practical concept for digital speakers to date, but quite a few contributions have been made that make the implementation of a digital power amplifier seem possible [3], [6], [8], [9], [11], [12]. The key to digital power amplification can be found in the PWM process.

Commercial audio amplifiers utilizing PWM have been successfully designed and – even if only for special applications – marketed [4], [17]. Those amplifiers are called Class-D amplifiers. However, the Class-D concept leaves it as an option whether to choose an analog or a digital modulator design, resulting in an analog or digital Class-D amplifier, respectively. To the best of the authors' knowledge completely specified, purely digital Class-D amplifiers are not yet commercially available today, due to many partly unsolved technical problems, some of which will be addressed in the subsequent chapters of this paper. A simplified block diagram of a Class-D amplifier is shown Figure 0.1. A low power audio input signal, which may be analog or digital PCM is fed into a pulse-width modulator. The resulting binary PWM-waveform is then power amplified. The amplified PWM-signal is applied to the demodulation system. The demodulation results in a power amplified audio signal.

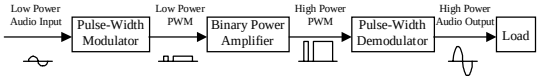


Figure 0.1 Basic Structure of a Class-D Audio Amplifier

The most important feature of such a system is the easy power amplification: As only a binary signal has to be amplified, the power amplifier reduces to a high power DC voltage source and a switch which is

controlled by the low power PWM-signal obtained from the pulse-width modulator. A more technical system diagram is shown in Figure 0.2. Herein an LC-low pass takes the place of the PWM-demodulator and the resistor R_L serves as load, which is typically a loudspeaker.

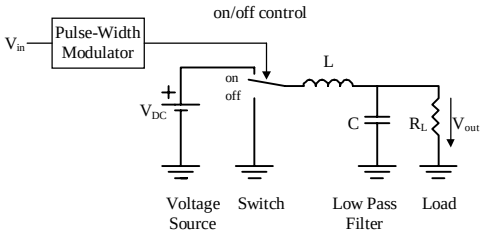


Figure 0.2 Functional Model of a Class-D Amplifier

In an actual system, the switch would be built using two fast switching power MOSFETs. In order to avoid a DC-offset across the load in the quiescent operating point, an H-bridge configuration would have to be used.

Two important advantages of the Class-D concept over the conventional Class-A/AB/B techniques should be mentioned here. First, the efficiency of a Class-D amplifier can theoretically reach 100%, as no other element in the power section of the system than the (resistive) load dissipates power. Ideally no heat sinks are required for the transistors that form the switch, because in the on- or off-state either the voltage across the device or current through it is zero, forcing the product of both – which equals the dissipated power – to zero. Hence, the Class-D technology offers small-size, low-cost high power audio amplification. Second, Class-D amplifiers are free of crossover distortion, which can be observed particularly in Class-B designs.

1 ANALOG AND DIGITAL PWM

The trailing edge natural pulse-width modulator (NPWM) shown in Figure 1.1 can be considered a classical PWM circuit. It consists of a sawtooth waveform generator and a voltage comparator. The fixed frequency of the sawtooth generator is set to a value that is large in comparison to the highest possible input signal frequency. The sawtooth frequency directly determines the pulse rate of the PWM signal. Sample timing diagrams for input and output signals are shown in Figure 1.2.

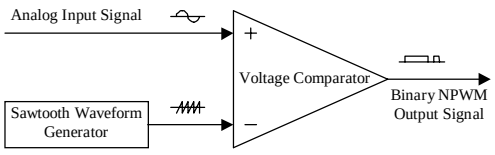


Figure 1.1 Functional Model of a Trailing Edge Natural Pulse-Width Modulator

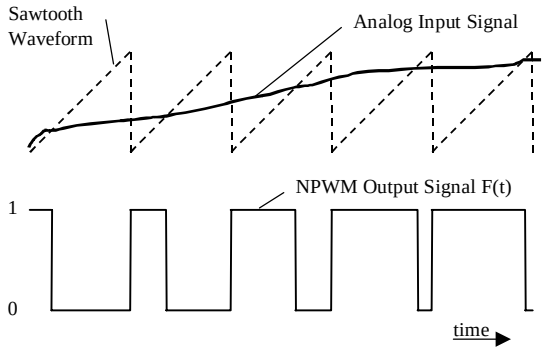


Figure 1.2 Trailing Edge NPWM Sample Timing Diagrams

In order to explain theoretically the PWM-based Class-D amplification, the spectrum of the PWM signal must be examined, because the spectrum of the analog output signal of a Class-D amplifier equals the spectrum of the PWM-signal after low-pass filtering in the PWM-demodulator. The spectra of the various kinds of PWM signals for single frequency sinusoidal input signals have been analytically determined using a two dimensional Fourier series. Decomposition of the unity-amplitude trailing edge NPWM-output signal for modulation by $M\cos\omega_v t$ into sinusoidal parts yields [1]:

$$F(t) = k + \frac{M}{2}\cos\omega_v t + \sum_{m=1}^{\infty}\frac{\sin m\omega_c t}{m\pi} - \sum_{m=1}^{\infty}\frac{J_0(m\pi M)}{m\pi}\sin(m\omega_c t - 2m\pi k) - \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{n=\pm\infty}\frac{J_n(m\pi M)}{m\pi}\sin(m\omega_c t + n\omega_v t - 2m\pi k - \frac{n\pi}{2})$$

Equation 1.1

The amplitude of the NPWM waveform is assumed to be unity. The variable ω_v is the angular input signal frequency, ω_c is the angular fundamental frequency of the PWM carrier, and k is the average amplitude of the unmodulated carrier. J_x denotes a Bessel function of first kind.

The spectrum consists of the input frequency, the carrier and its multiples, and the sums and differences of the input signal and the carrier and its multiples. It is very important to realize that there are no harmonics of the input signal. However, the modulation products of the input signal and carrier fall back towards the input signal frequency, even though their amplitudes decrease. Thus, the carrier frequency should be much higher than the highest input frequency in order to have negligible modulation products affecting the audio base band. In practical PWM designs that cover the whole audio band of DC to 20kHz, the PWM carrier often is in the range of 200 to 300kHz [4], [13], [17]. A sample NPWM spectrum is shown in Figure 1.3.

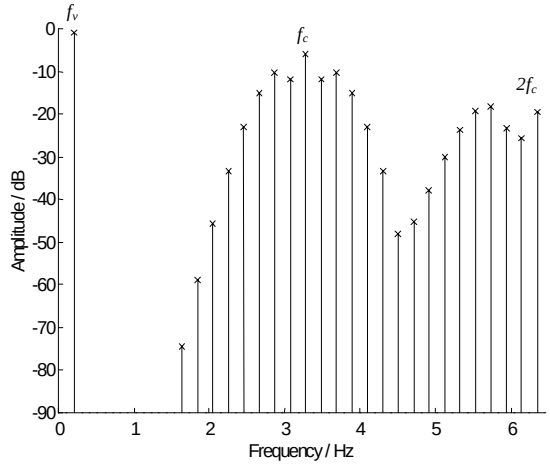


Figure 1.3 Sample Trailing Edge NPWM Spectrum

The PWM output of analog modulators, such as the one described previously, is continuous in time, but has discrete amplitude values. It is certainly possible to introduce some sort of pulse-width quantization such that the PWM-signal resembles a one bit digital signal which is discrete in time and amplitude. Next, it seems to be reasonable to look for a direct way to convert digitally a uniformly sampled digital PCM signal, such as music from a CD-player, into a digital PWM-signal, which can then be power amplified. A device that does this can be called a power digital-to-analog converter (DAC), or a digital power amplifier. The PCM-to-PWM converter can be called a digital pulse-width modulator. It is important to state that direct PCM-to-PWM conversion is not equivalent to using a conventional digital-to-analog converter and feeding its output signal into an analog pulse-width modulator, like the one described previously.

A digital pulse-width modulator is a device that converts amplitude samples into pulses with proportional width. This can be done with a simple counting circuit, such as the one depicted in Figure 1.4.

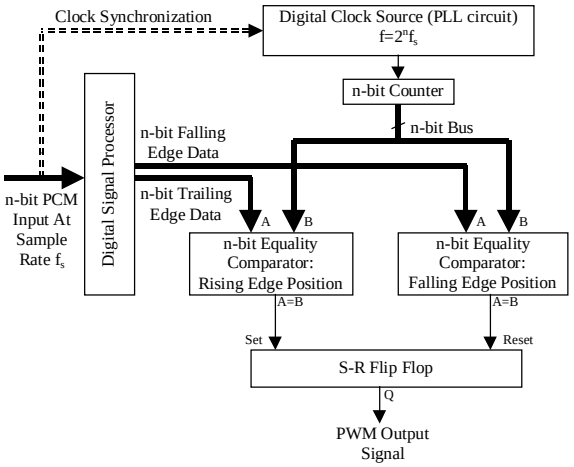


Figure 1.4 System Diagram of an n-Bit Digital Pulse-Width Modulator

This circuit allows independent modulation of the leading and trailing edge. The digital signal processor (DSP) determines what kind of modulation is performed. In the simplest case, an incoming PCM sample would be directly used to set the position of the leading or trailing edge of the corresponding PWM pulse, and the other edge has a fixed position. The direct mapping of PCM samples into pulse-widths is commonly called Uniform Pulse-Width Modulation (UPWM) [6]. In the following paragraphs, two UPWM versions will be introduced that have special importance in this context.

A functional model of a trailing edge uniform pulse-width modulator is shown in Figure 1.5. Sample timing diagrams are shown in Figure 1.6.

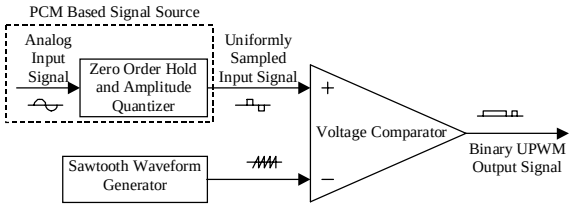


Figure 1.5 Functional Model of a Trailing Edge Uniform Pulse-Width Modulator

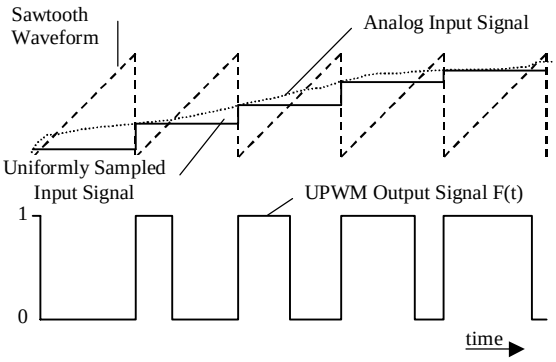


Figure 1.6 Trailing Edge UPWM Sample Timing Diagrams

The trailing edge UPWM signal can be decomposed as follows [1]:

$$F(t) = k - \sum_{n=1}^{\infty} \frac{J_n\left(\frac{n\pi M\omega_r}{\omega_c}\right)}{\frac{n\pi\omega_r}{\omega_c}} \sin\left(m\omega_r t - \frac{2n\pi k\omega_r}{\omega_c} - \frac{n\pi}{2}\right)$$

$$+ \sum_{m=1}^{\infty} \frac{1 - J_0(m\pi M)}{m\pi} \sin m\omega_c t$$

$$- \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{n=\pm\infty} \frac{J_n\left[\left(m\omega_c + n\omega_r\right)\frac{\pi M}{\omega_c}\right]}{\left(m\omega_c + n\omega_r\right)\frac{\pi}{\omega_c}} \sin\left(\left(m\omega_c + n\omega_r\right)\left(t - \frac{2\pi k}{\omega_c}\right) - \frac{n\pi}{2}\right)$$

Equation 1.2

As can be seen from the first sum in the above equation, the spectrum contains harmonics of the modulating frequency. The amplitudes of those harmonics increase with modulation index and modulating frequency. Linear approximations for the

harmonic amplitudes can be found in [6]. Furthermore, the spectrum contains multiples of the carrier and sums and differences of carrier and modulating signal frequency. A sample spectrum is shown in Figure 1.7.

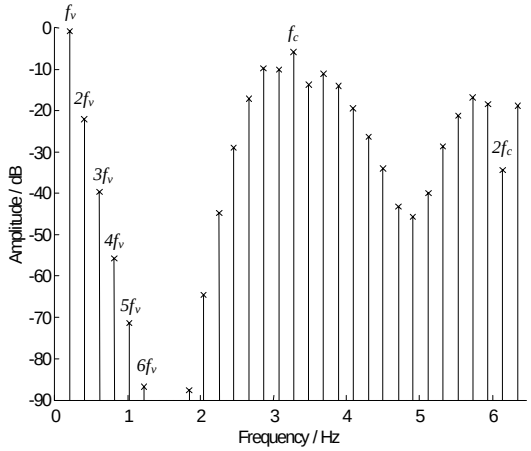


Figure 1.7 Sample Trailing Edge UPWM Spectrum

A functional model of a double-sided uniform pulse-width modulator is shown in Figure 1.8. Sample timing diagrams are shown in Figure 1.9. There are two forms of double-sided UPWM having either one or two input samples per pulse. In the latter case, each edge is be modulated independently by a different sample. However, for this paper only UPWM with one sample per pulse is considered.

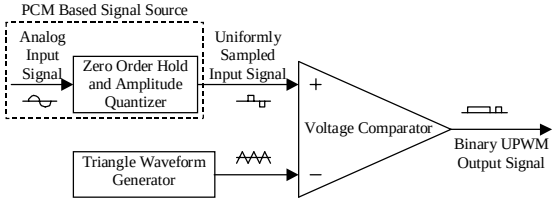


Figure 1.8 Functional Model of a Double-Sided Uniform Pulse-Width Modulator

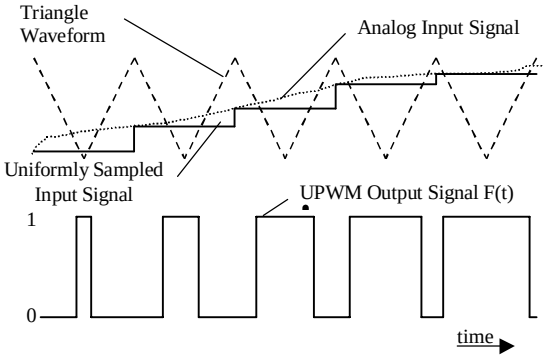


Figure 1.9 Double-Sided UPWM Sample Timing Diagrams

The double-sided UPWM signal can be decomposed as follows [1], [12]:

$$F(t) = k + \sum_{n=1}^{\infty} \frac{2J_n\left(\frac{M\pi n\omega_c}{2\omega_c}\right)}{\pi n\frac{\omega}{\omega_c}} \sin\left(n\left(1-\frac{\omega_c}{\omega_c}\right)\frac{\pi}{2}\right)\cos\left(n\omega t - \pi n\frac{\omega_c}{\omega_c}\right)$$

$$+ \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{2J_n\left(\frac{M\pi n\omega_c}{2\omega_c}\right)}{\pi\left(m+n\frac{\omega}{\omega_c}\right)} \sin\left(\left(m+n\left(1-\frac{\omega_c}{\omega_c}\right)\right)\frac{\pi}{2}\right)\cos\left(n\omega t + m\omega_c t - \pi n\frac{\omega_c}{\omega_c}\right)$$

Equation 1.3

The double-sided UPWM is also characterized by a harmonic content in the base band. And again, modulation products of carrier and input signal are present. A sample spectrum shown in Figure 1.10. Notice that the baseband harmonics drop off faster for double-sided UPWM than for trailing edge UPWM (Figure 1.7).

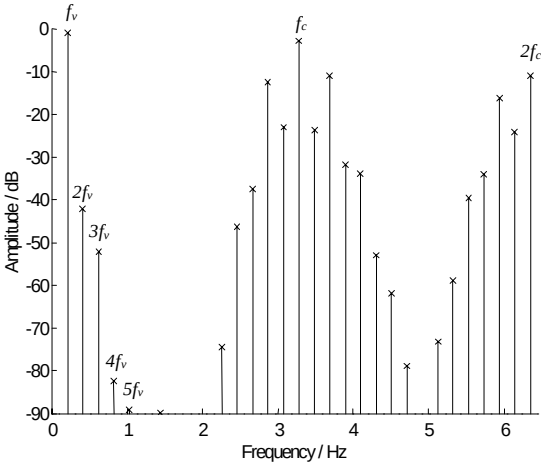


Figure 1.10 Sample Double-Sided UPWM Spectrum

2 PWM LINEARIZATION TECHNIQUES

As mentioned in the previous section, a direct conversion of uniformly sampled PCM data into PWM data would result in a high harmonics content in the audio band, inhibiting high-fidelity applications. Therefore, the PCM data must be predistorted before they are fed into the PCM-to-PWM conversion process, such that the PWM-nonlinearities are compensated. A signal flow graph is shown in Figure 2.1. In the last fifteen years a couple of linearization methods have been developed by various researchers [3], [6], [8], [9], [11], [12].

Two methods that were be implemented in a C67-based real-time DSP system – Pseudo Natural PWM, and Dynamic Filtering – will be described in more detail. A third approach which is based on a totally different modulation concept called click modulation will be outlined. A brief system design for a click modulator will be introduced in this chapter. Finally, a fourth method called Nonlinear Noise Shaping will be mentioned only for reference purposes.

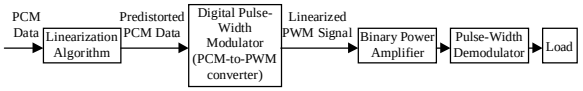


Figure 2.1 Basic Structure of a Linearized Digital Class-D Audio Amplifier

2.1 Pseudo-Natural PWM

PNPWM was introduced by Goldberg and Sandler [6]. The basic idea is to mimic NPWM, based on uniform PCM data. Recall that NPWM signals are free of harmonics in the baseband, as described above. This strategy is depicted in Figure 2.2 for a single PWM pulse.

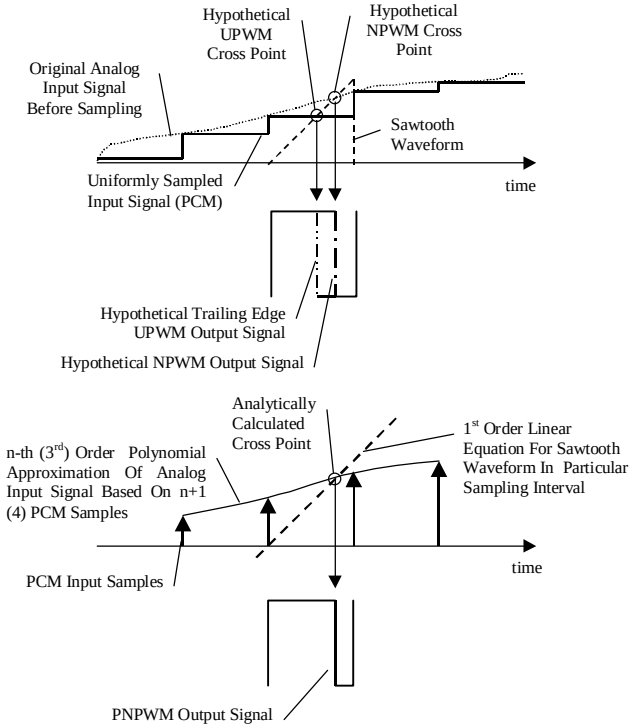


Figure 2.2 PNPWM Sample Timing Diagrams

In order to calculate the cross point of the sampling sawtooth with the analog signal based on its PCM samples, a continuous reconstruction of the analog signal is necessary in the time interval of the particular PWM pulse. In accordance with the sampling theorem, this would have to be done using a sinc-function-based approach incorporating all PCM samples prior to the interval and after it [14]. That means, an accurate analytical expression for the reconstructed analog input waveform would consist of an infinite number of scaled and time shifted sinc-functions. The sampling sawtooth waveform can be described as a first-order equation. Next, the cross point of the reconstructed signal with the sampling sawtooth would have to be determined by solving a system of the two corresponding simultaneous equations.

However, a more practical way is to approximate the analog waveform by an n-th order polynomial using n+1 PCM samples from both sides of the interval to be reconstructed. The higher the order of the approximation polynomial the smaller is the error. In order to avoid having to solve the resulting higher-order equation system analytically, a numerical algorithm such as the Newton-Raphson method can be employed.

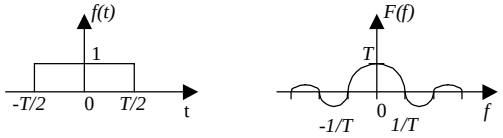
The PNPWM method is a very powerful means of correcting the harmonics content in the base band, but the NPWM characteristic sum and difference tones of modulating signal and carrier, which fall back into the base band are not eliminated. Therefore, PNPWM can be applied only in conjunction with a high carrier frequency of at least four times the audio sample rate.

2.2 Dynamic Filtering

Another linearization approach has been suggested by Hawksford [8], [9]. It is particularly well-suited for double-sided UPWM signals which, were described in Section 1. The method can be called dynamic filtering.

A brief investigation of the UPWM-inherent nonlinearities is necessary to understand the dynamic filtering method. It is easiest to find the origin of the nonlinear behavior by comparing a PCM signal, which is free of harmonics, and a PWM signal generated by direct amplitude-to-pulse-width mapping from the same PCM signal, keeping in mind that the demodulation in both cases is done by low-pass filtering. This comparison is done on a sample-by-sample basis in the frequency domain. Recall the Fourier transform for a rectangular pulse is

$$f(t) = \mathrm{rect}(\frac{t}{T}) \xleftrightarrow{FourierTransform} F(f) = T\,\mathrm{sinc}(fT)$$



Equation 2.1

Now consider a three-sample PCM-sequence and a three-sample PWM-sequence and the Fourier transforms of each individual pulse:

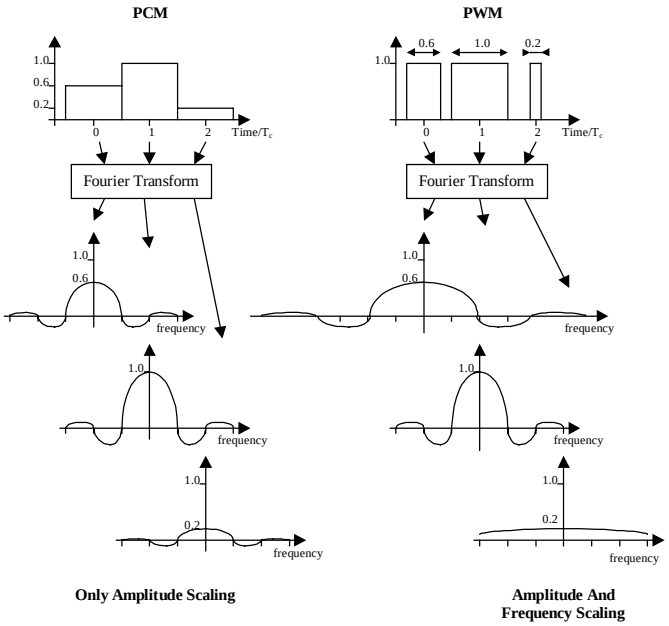


Figure 2.3 PCM-PWM Spectra Comparison

As is apparent from the above equation and Figure 2.3, the transfer function of a PCM system is constant, since each PCM sample has the same spectrum, which is only amplitude scaled. The individual PWM samples, however, have different Fourier transforms with respect to amplitude and frequency scaling. Therefore, a PWM system can be thought of as a PCM system with a time-varying transfer function. In order to linearize the PWM system, an equalizing filter is needed that compensates the sample-dependent changes. The transfer function of this filter would, therefore, have to change from sample to sample, forcing the overall transfer characteristic to be constant at least in the audio baseband. This is depicted in Figure 2.4.

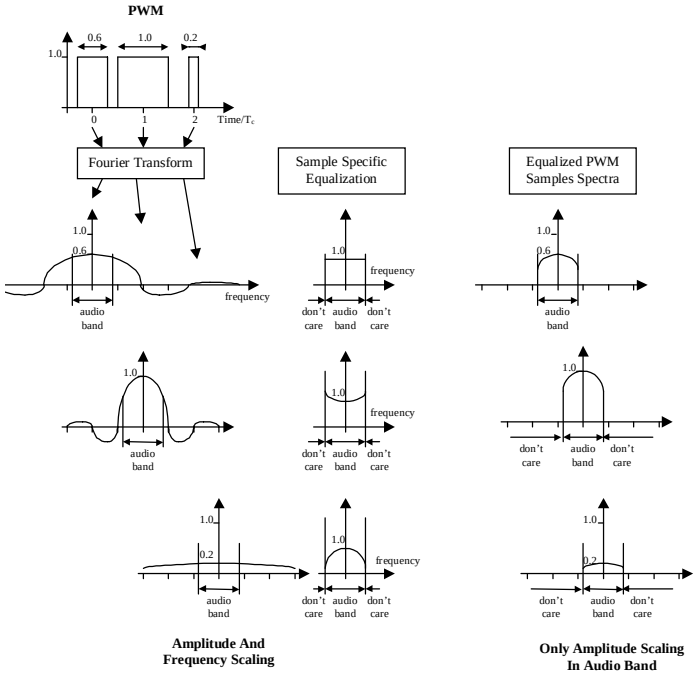


Figure 2.4 Frequency Domain Analysis of Dynamic PWM-Linearization

Each sample has its own 4th-order FIR equalization filter, whose magnitude response would have to be the approximate inverse of the PWM sample's frequency spectrum, such that product of both is unity, at least in the audio band. However, following Hawksford [8], [9], a flat overall response will not be targeted, but the spectrum that corresponds to 50% duty cycle PWM-pulse.

Each of those sample specific 4th-order FIR equalization filters has a dispersive response, affecting the two previous and the two following PWM-samples, thereby changing their values and then their associated equalization filters, which affect the initial PWM sample again. It is obvious that the sample-based equalization method relies on a convergence after a certain number of iteration steps. Therefore, a number of samples and their specific equalization filters interact to produce the overall dynamic PWM linearizing filter.

Finally, it must be said that according to simulation results, a modest oversampling is required for the dynamic filtering method. A ratio of four yields good results as described in Section 4.2.

2.3 Click Modulation

The click modulation technique was introduced by Logan in 1984 [11]. The analytic derivation of this technique is far too complex to be shown in this paper. Click modulation allows the generation of a width-modulated pulse stream, whose spectrum has a separated base band, as opposed to the modulation techniques discussed in Section 1. Most importantly, a click modulated pulse stream does not require any oversampling, and satisfies the minimum requirements of the sampling theorem. Click modulation-based PWM seems very well suited for digital power amplification, as it results in the theoretically minimal pulse rate thereby lowering the speed requirements of the power switch elements and the digital modulator clock. However, the drawbacks of this technique are outrageous signal processing speed requirements, and very sharp PWM-demodulator filters, which will necessarily introduce comparatively high amplitude, and phase ripple. Both obstacles can be overcome by using newest generation DSP technology and the application of an adaptive filter as described in Section 6. An analog click modulator system is shown in Figure 2.5.

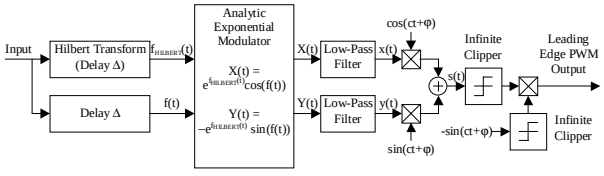


Figure 2.5 Click Modulator

At the input to the click modulator a Hilbert transform of the band-pass audio signal has to be performed. The Hilbert transform - which is basically a 90° phase shift for all frequencies - can be performed using IIR filters, FIR filters, or a sliding FFT (SFFT) [19]. In this context, an FIR solution seems best suited, as a perfect 90° phase shift is guaranteed [14], because an FIR filter with odd impulse response has a purely imaginary frequency response. In order to obtain a maximally flat magnitude response, the Parks-McClellan algorithm can be used for the filter design [14]. Simulations showed that a 0.01dB amplitude ripple over the entire audio band from 20Hz to 20kHz must not be exceeded in order to satisfy today's digital audio requirements with SNRs of at least 96dB. The order of the Hilbert transform FIR filter is therefore very high (a few thousands). However, a multi-rate filterbank can be used to break up the transform task into multiple frequency bands, where lower order FIR filters yield sufficient performance. A sample 3-band filter bank is shown in Figure 2.6. The basic idea of such a filter bank is to perform the Hilbert transform over only a small band such as one decade (2kHz...20kHz) with a single FIR filter. Simulations show that a filter order of less than 50 is sufficient to guarantee the required linearity of the magnitude response. The next lower decade (200Hz...2kHz) of the input bandwidth would be covered with another Hilbert transforming FIR filter with the same order, but at only one tenth of the sampling rate. Similarly, the last decade (20Hz...200Hz) could be transformed independently. The three different bands have to be added after bringing the outputs to same sampling rate. It is important to use linear phase FIR filters for the sample rate conversion processes such that no additional phase shifts are introduced. Furthermore, the Hilbert transform filters should cover a little more than just the bands indicated in Figure 2.6, in order to guarantee proper operation also in the transition bands of the stages. The structure shown in Figure 2.6 can certainly be optimized and extended to cover an even wider frequency range with a smaller or bigger number of processing-bands. However, care must be taken considering the noise performance of a system with many digital filters.

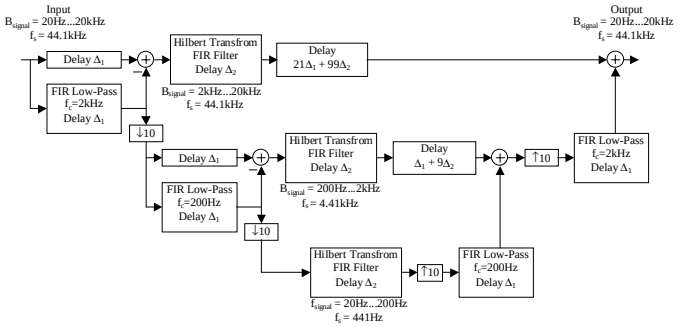


Figure 2.6 Hilbert Transform Filter Bank

The next subsystem of the click modulator is the Analytic Exponential Modulator. Exponential, and sine and cosine operations have to be performed in that stage. Clearly, this introduces harmonics to the input signal. In a digital implementation aliasing will inevitably occur unless the sample rate is infinite. However, as the harmonic amplitudes drop rapidly at higher frequencies, a four times oversampled process yields good results. The succeeding low-pass filters are operated at the higher rate, too (4*44.1kHz), and have a transition band of 20kHz...22050kHz. The stop band attenuation should be larger than 96dB for CD-quality results. The system simulated to obtain the plot shown later on used 500th order linear phase FIR filters.

Both low-pass signals are now multiplied with cosine and sine functions of half the PWM-carrier frequency (c = π*44.1kHz). Clearly, the resulting signal is now confined to the bandwidth 0...44.1kHz, such that at least a 88.2kHz sampling frequency is required for this processing step, which results in the intermediate signal s(t).

Finally, in an analog click modulation system clipping and multiplying operations have to be performed in order to obtain the PWM output signal. It is very important to notice, that the information of the input signal is coded into the position of zero crossings of the signal s(t) relative to the PWM-clock signal -sin(ct). It can be shown that the signal s(t) has exactly one zero-crossing in each halfwave of -sin(ct). The PWM-output changes its level where the zero-crossings of either -sin(ct), or s(t) occur. This is depicted in Figure 2.7 for continuous signals.

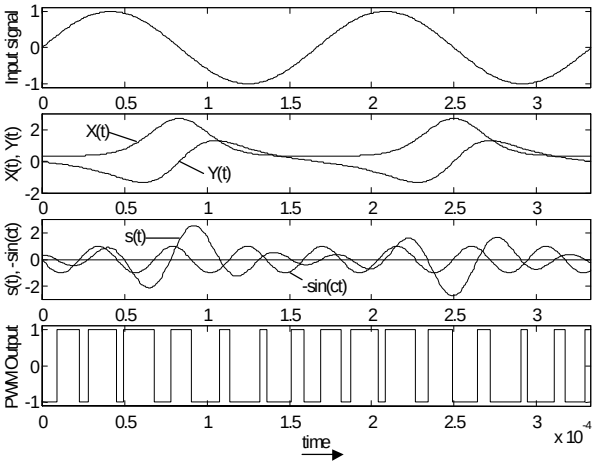


Figure 2.7 Click Modulation Timing Diagrams (6kHz Input Frequency, 44.1kHz PWM Carrier Frequency)

In a digital system, however, -sin(ct) and s(t) would exist as sampled waveforms. The signal –sin(ct) is generated by the digital system and its zero-crossings would be known. But in order to obtain a high-resolution (16-bit) PWM, s(t) would have to be sampled at 2^{16}*44.1kHz, as only then the zero-crossing positions could be determined with the sufficient accuracy. A computationally more efficient way is to have a much lower sampling rate – the bandwidth of s(t) is limited to 0...44.1kHz, as mentioned above – and find the zero-crossings with technique similar to the one used in PNPWM. A number of sample points of s(t) surrounding the zero-crossing of interest can be taken, an approximation polynomial can be fitted, and its zero-crossing can be found analytically, or using the Newton-Raphson technique. This is depicted in Figure 2.8 for s(t) sampled at 4*44.1kHz and a 7th order approximation polynomial. The corresponding PWM output spectrum, which was generated with MATLAB [20], is shown in Figure 2.9. The input frequency was 6kHz and the PWM carrier frequency 44.1kHz. The PWM resolution was only limited by MATLAB's internal 64-bit word length. The spectrum, which was computed with a rectangular window FFT, shows that all harmonics are well below 96dB.

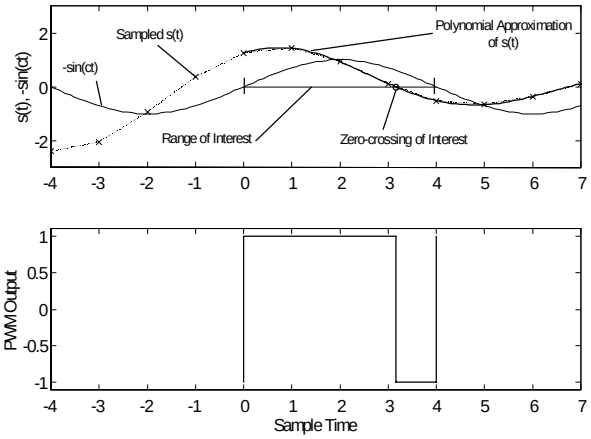


Figure 2.8 Polynomial Approximation of s(t) and Resulting PWM-Pulse

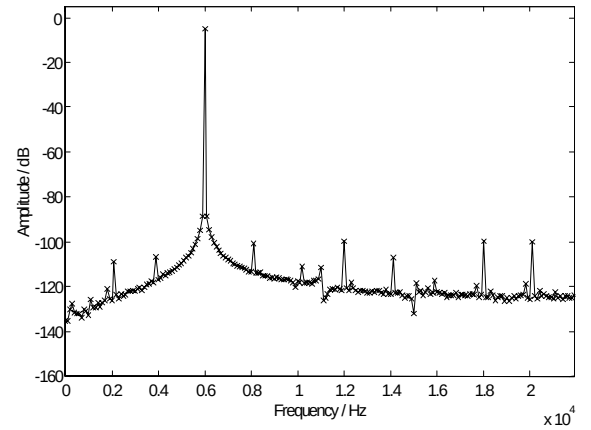


Figure 2.9 Click Modulation Output Spectrum

A system design for a digital click modulator is shown in Figure 2.10.

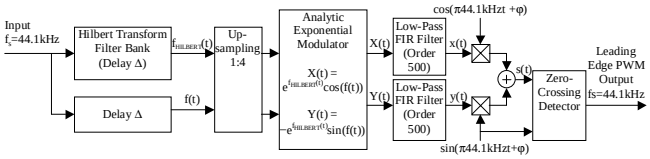


Figure 2.10 Digital Click Modulator System

A real time implementation of the click modulator would most probably require a multi-processor solution – even with today's advanced DSP technology. It will be left to future research to experimentally verify this technique.

2.4 Nonlinear Noise Shaping

Another way to linearize PWM generated by uniformly sampled PWM data was proposed by Craven [3]. This technique utilizes a special nonlinear noise shaping network. However, the system is based on high oversampling ratios, resulting in high pulse-rates, which are disadvantageous to the Class D power amplifier concept. This is because the switching speed of the MOSFETs in the binary power amplifier stage is limited. However, the nonlinear noise shaping approach may very well be used for low power PWMDAC applications [18].

3 DIGITAL CLASS-D AMPLIFIER SYSTEM DESIGN

A signal flow graph of an entirely digital Class-D amplifier is shown in Figure 3.1.

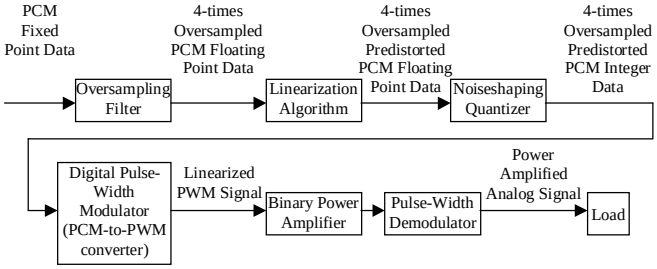


Figure 3.1 Signal Flow Graph of a Digital Power Amplifier

Two additional system components were introduced: An oversampling filter, and a noise shaping quantizer. The design of oversampling filters is not very problematic and will therefore not be described in this text. Detailed information can be found in [14]. The application of a noise shaping quantizer is necessary in order to obtain n-bit fixed point data which can be fed into the PCM-to-PWM converter. Furthermore, noise shaping allows utilizing the excess bandwidth gained through oversampling to increase the audio band signal-to noise ratio (SNR) of the system. Various design methods of noise shaping quantizers have been described in [5], [7], [16], [21], and [22]. However, for this work the design algorithm suggested by Hallock and Tewksbury [16] was followed, and a 4^{th} order noise shaping filter was simulated and implemented. Finally, it must be said that the application of the above noise shaping structure is not 100% correct in a PWM-system, as pointed out by Craven [3]. Floating-point sample values coming from the PWM-linearizer reflect pulse-lengths rather than pulse-amplitudes. But the noise shaping filter design methods commonly used are based on the assumption that the samples to be quantized represent amplitude values. This discrepancy manifests itself in noise modulation products that fall back into the audio band, and increase the noise floor slightly. The noise shaping network mentioned in Section 2.4 was designed to avoid this effect.

One of the crucial issues of digital Class-D amplifiers is the open-loop structure [13]. In contrast to the analog Class-D amplifier, the digital amplifier cannot be easily encompassed by a feedback loop, because of the many delays introduced by the necessary ADC, its associated signal conditioning filters, and the linearization filter, as shown in Figure

3.2. Problems which would be more easily solved with a feedback loop include the introduction of distortion by a nonideal power switch and demodulator low pass filter, the load dependent transfer characteristic of the demodulation low-pass, and the highly accurate stabilization of the high-power DC H-bridge voltage-supply. The latter problem is especially important, because the open-loop Class-D amplifier has a 0 dB power supply rejection ratio (PSRR).

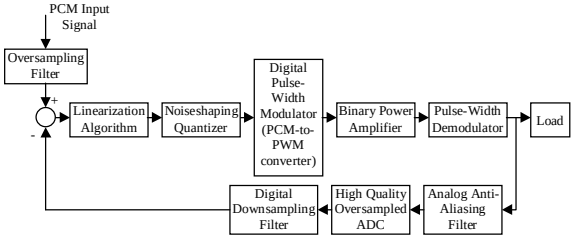


Figure 3.2 Hypothetical Digital Class-D Amplifier with Feedback Loop

4 SIMULATION RESULTS

A digital Class-D amplifier using both of the two PWM linearization methods described above was modeled and simulated using the MATLAB SIMULINK system [20]. A detailed description of the model used can be found in [2]. The plots in the following subsections show the spectra of the PWM output signals with and without linearization, and noise shaping. They were calculated using a Fast Fourier Transform (FFT) with rectangular window. Also, the effects of a limited (10-bit) PWM resolution were simulated as opposed to a full 64-bit precision, which marks the limit of the capabilities of the MATLAB SIMULINK system.

4.1 Pseudo-Natural PWM

The output spectra for a 6 kHz, 90% full-scale input signal, sampling frequency = 4 * 44.1kHz are shown below:

	PWM Resolution	Noise Shaper	Linearizer
Figure 4.1	Full	N/A	Off
Figure 4.2	Full	N/A	On
Figure 4.3	10 Bit	Off	On
Figure 4.4	10 Bit	On	On

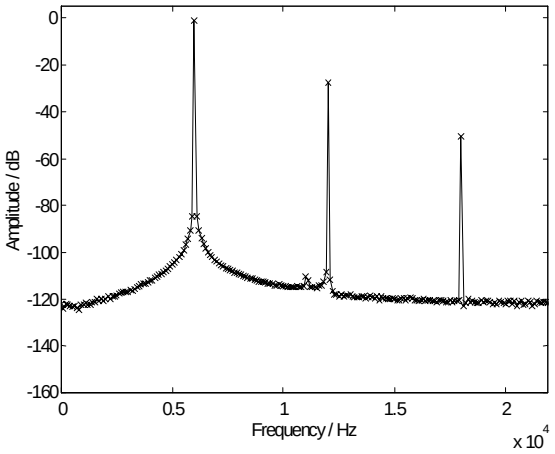


Figure 4.1 Full-precision Trailing-edge UPWM, No Linearization

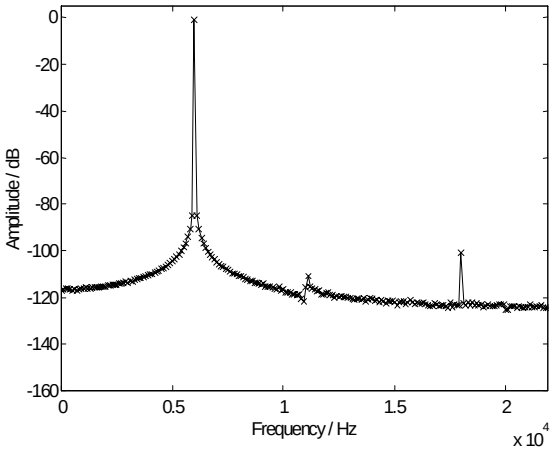


Figure 4.2 Full-precision Trailing-edge UPWM, PNPWM Linearization (3rd-order Polynomial)

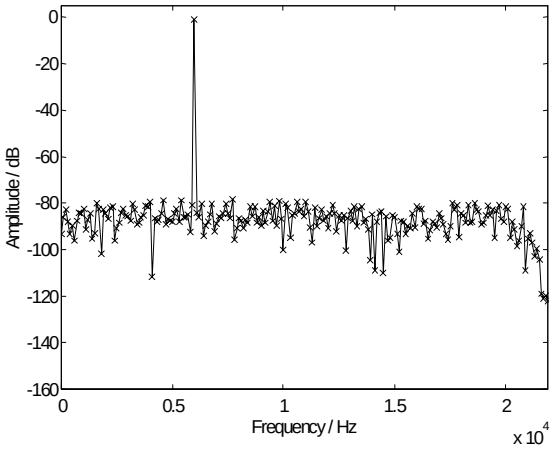


Figure 4.3 10-bit Trailing-edge UPWM, PNPWM Linearization (3rd-order Polynomial), No Noise Shaping

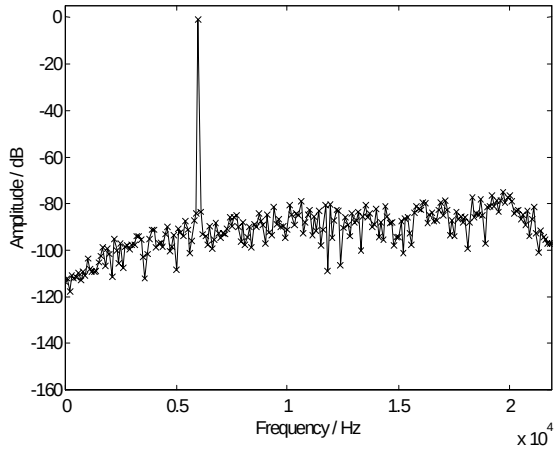


Figure 4.4 10-bit Trailing-edge UPWM, PNPWM Linearization (3rd-order Polynomial), 4th-order Noise Shaper

Comparing Figure 4.1 and Figure 4.2 the effect of the PNPWM linearizer can be easily recognized, as the amplitude of the harmonics of the input signal decrease significantly. Even though only a 3rd order approximation polynomial was used, the harmonics amplitude is well below 90dB. Figure 4.3 and Figure 4.4 show the PWM spectra for a limited pulse-width resolution. As expected the noise floor rises with limited PWM resolution. The effect of the noise shaping quantizer can be observed in Figure 4.4, as the noise floor drops towards lower frequencies.

4.2 Dynamic Filtering

The output spectra for a 6 kHz, 90% full-scale input signal, sampling frequency = 4 * 44.1kHz are shown below. The order of the sample specific equalization filters was 4. 6 adjacent interacting PWM samples formed the dynamic linearizing filter.

	PWM Resolution	Noise Shaper	Linearizer
Figure 4.5	Full	N/A	Off
Figure 4.6	Full	N/A	On
Figure 4.7	10 Bit	Off	On
Figure 4.8	10 Bit	On	On

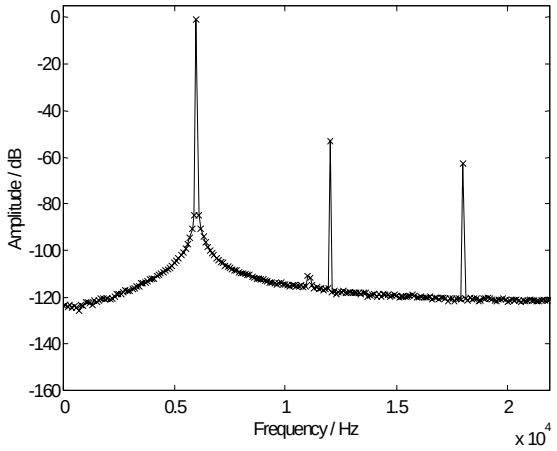


Figure 4.5 Full-precision Double-sided UPWM, No Linearization

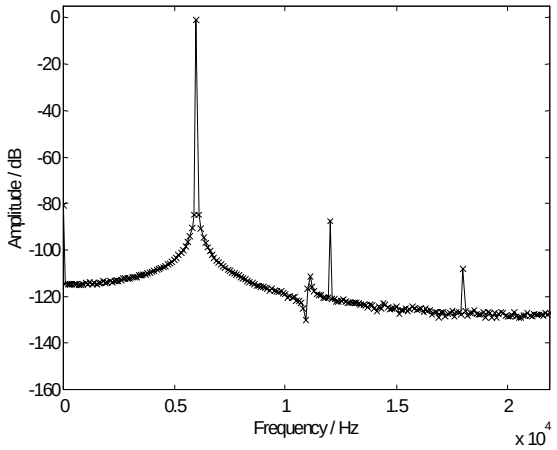


Figure 4.6 Full-precision Double-sided UPWM, with Dynamic Filter

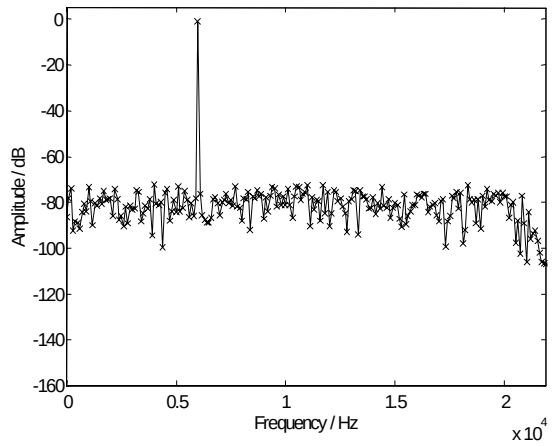


Figure 4.7 10-bit Double-sided UPWM, No Noise Shaping, with Dynamic Filter

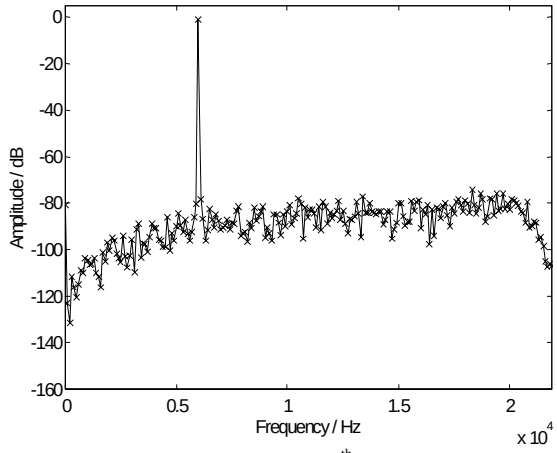


Figure 4.8 10-bit Double-sided UPWM, 4th-order Noise Shaper, with Dynamic Filter

Also the simulation results for the dynamic filtering linearization show that the proposed method works. The frequency spectra are very similar to those shown in Section 4.1.

5 IMPLEMENTATION

5.1 System Description

The laboratory prototype, which was built to verify the proposed linearization algorithms, comprises many individual subsystems that were built around the digital pulse-width modulator. A picture of the setup is shown in Figure 5.1.

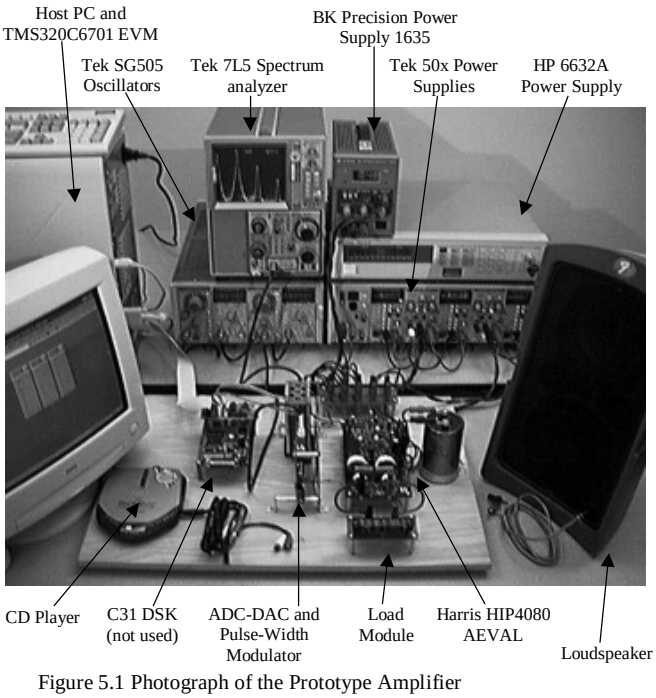


Figure 5.1 Photograph of the Prototype Amplifier

A signal flow graph is shown in Figure 5.2. The audio input to the system is shown on the left. There is a digital input using either a standard TOSLINK interface, or an electrical coax connector. Alternatively, there are two analog inputs, which are summed using an ultra low distortion opamp circuit built with Burr-Brown OPA4134 devices. The analog sum signal is fed into a Crystal Semiconductor CS5360 24-bit Sigma-Delta ADC. Either input signal can be manually selected by the user to be fed into the TMS320C6701EVM DSP via an opto-isolated serial interface. The selected signal is simultaneously converted back to analog using a Crystal Semiconductor CS4335 24-bit Sigma-Delta DAC in order to allow direct evaluation of the noise and distortion performance of the input circuitry, and can be obtained at connector J1/J2.

The signal processing steps, such as oversampling, linearizing, and noise shaping are performed in the TI TMS320C6701. It must be mentioned that an additional prefiltering step is necessary, as the CS5360 causes aliasing for high frequency input signals. The real-time software was written in C and linear assembly, because the both linearization algorithms are computationally very intensive and have to be performed at four times oversampled speed.

The linearized PWM-data is transmitted to a counting circuit, which performs the digital PWM as described in Section 1. The modulator has a 10-bit pulse-width resolution requiring a clock frequency of 2^{10}*4*44.1kHz = 181MHz for CD-standard PCM signals brought in via the TOSLINK interface. Building a digital circuit that runs at speeds higher than 100MHz is quite challenging, as no standard logic family would be fast enough. Also, reasonably priced high density FPGAs are not capable operating at such high speed. In order to avoid an ECL solution, which is rather inconvenient due to amount of circuitry needed, a low density PLD approach was chosen using eight Lattice Semiconductors GAL22V10-LJ4 chips. Those Generic Logic Array (GAL) devices contain 10 flip-flops and a large number of electrically configurable gates. The particular type used has a specified propagation delay of 4ns. Unfortunately, there seemed to be no other way than using PECL devices for the clock generation for the pulse-width modulator. The PLL used is a Synergy Semiconductors SY89421V chip.

The digital PWM signal is then fed into an H-bridge module HIP4080AEVAL by Harris Semiconductors. The HIP4080AEVAL is actually a complete analog Class-D amplifier evaluation board, whose analog pulse-width modulator was disabled for this application. The H-bridge drives a 4Ω load through a 4thorder LC-Butterworth low-pass filter. The voltage across the load is measured, digitized and also fed into the DSP for a future extension of the system, which will be described in Section 6.

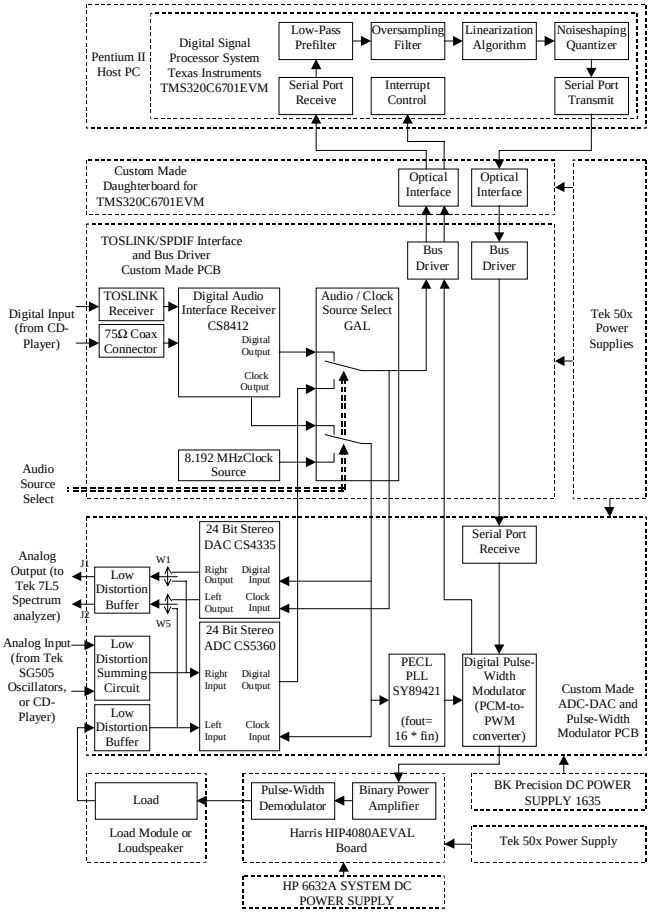


Figure 5.2 Prototype Amplifier Signal Flow Graph

5.2 Measurement Results

The experiments conducted follow the simulations of Chapter 4. However, the simulations were carried out having a system sampling frequency of 4*44.1 kHz, whereas the amplifier prototype ran at 4 * 36.6 kHz. The 10-bit PWM signal was obtained at the TTL output of the pulse-width modulator. The analog input signal was generated with a Tektronix SG505 oscillator. The output spectra were recorded with an analog Tektronix 7L5/7603 spectrum analyzer.

5.2.1 Pseudo-Natural PWM

The output spectra for a 6 kHz, 90% full-scale input signal, 10-bit trailing edge uniform PWM, PNPWM linearizer with 3rd order polynomial, 4th order noise shaper are shown below:

	PNPWM Linearizer	Noise Shaper
Figure 5.3	Off	Off
Figure 5.4	On	Off
Figure 5.5	On	On

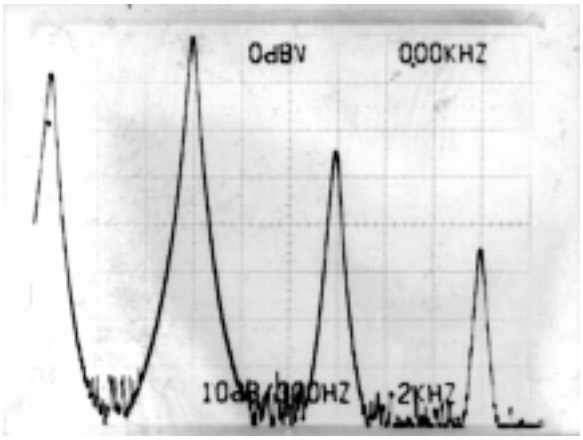


Figure 5.3 10-bit Trailing-edge UPWM, No Linearization, No Noise Shaping

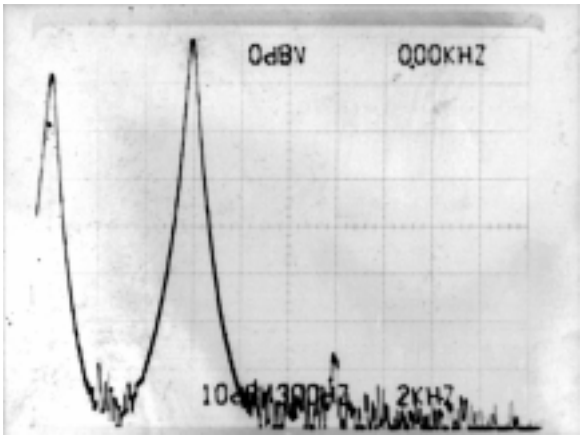


Figure 5.4 10-bit Trailing-edge UPWM, PNPWM Linearization (3rd-order Polynomial), No Noise Shaping

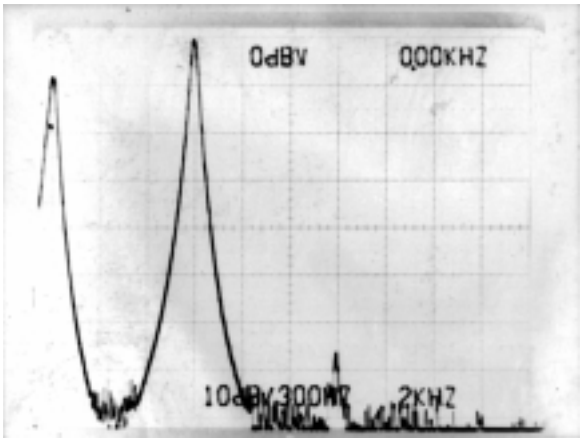


Figure 5.5 10-bit Trailing-edge UPWM, PNPWM Linearization (3rd-order Polynomial), 4th-order Noise Shaper

The experimental results validate the simulation. A significant reduction on the harmonic amplitudes can be observed. However, as opposed to the simulation, the laboratory prototype amplifier does not dither the floating point PWM output of the linearizer before rounding. The –65dB first harmonic residue in the

output signal spectrum can be attributed to the quantizing effects [5].

5.2.2 Dynamic Filtering Measurement Results

The output spectra for a 6 kHz, 90% full-scale input signal, 10-bit double-sided PWM, 6th-order dynamic filter with 4th-order equalizers, 4th-order noise shaper are shown below:

	Dynamic Filter	Noise Shaper
Figure 5.6	Off	Off
Figure 5.7	On	Off
Figure 5.8	On	On

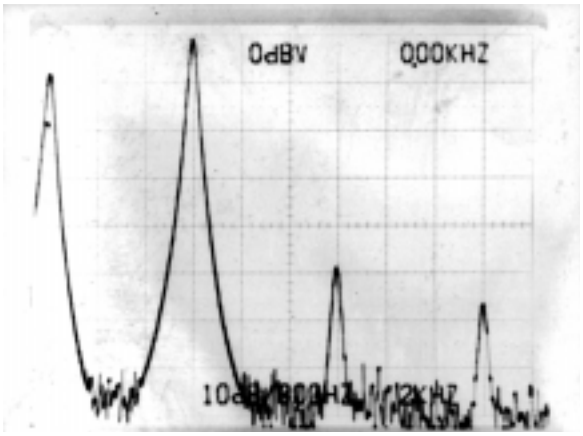


Figure 5.6 10-bit Double-sided UPWM, No Linearization, No Noise Shaping

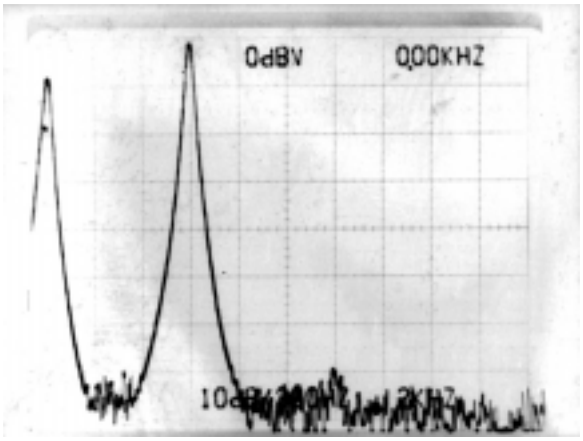


Figure 5.7 10-bit Double-sided UPWM, Dynamic Filter Linearization, No Noise Shaping

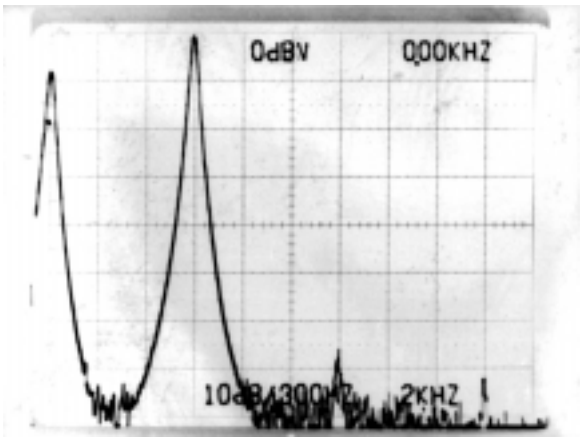


Figure 5.8 10-bit Double-sided UPWM, Dynamic Filter Linearization, 4th-order Noise Shaper

The experimental results for the dynamic filtering linearization also shown a drastic reduction of the harmonics content. However, also here the noise performance does not satisfy the stringent requirements of today's digital audio standards. A higher PWM-resolution will of course result in a better SNR performance, so that a modulator design with 16-bit resolution should be targeted. Such a design would have to be based on ECL technology, or even an ASIC solution.

Lastly, it must be mentioned that the power amplified PWM-signal showed a significant amount of distortion, which is reintroduced by the HIP4080AEVAL H-bridge and MOSFET driver chip. The redesign and optimization of the H-bridge is one of the topics of future research work.

6 ADAPTIVE FILTER EXTENSION

As an extension of the conventional system design approach for digital Class-D amplifiers (Figure 2.1), this paper proposes the application of an adaptive filter to ease some of the problems with open-loop designs. The modified system structure is shown in Figure 6.1.

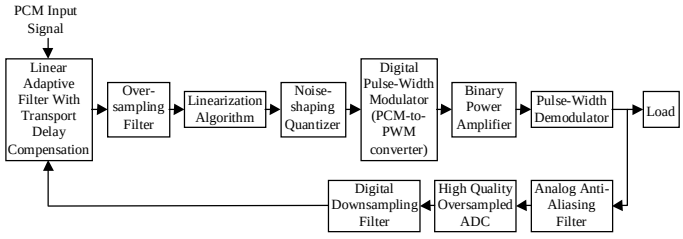


Figure 6.1 Signal Flow Graph of a Digital Class-D Amplifier with Linear Adaptive Filter

Another version of the above flow graph is shown in Figure 6.2. Here, the linearized Class-D amplifier system is simplified to a higher order linear system introducing a transport delay T_1. Furthermore, the delay caused by the feedback ADC is modeled as transport delay T_2. The transport delay compensation is done by introducing another delay T_3, where

$$T_3 \geq T_1 + T_2$$

Equation 6.1

It is important to realize, that in order to guarantee system stability, the update rate of the weights in the adaptive filter, and the coefficients of the additional FIR filter must not exceed $1/T_3$, because the weight update will affect the error E_{T3} after the time delay T_1+T_2.

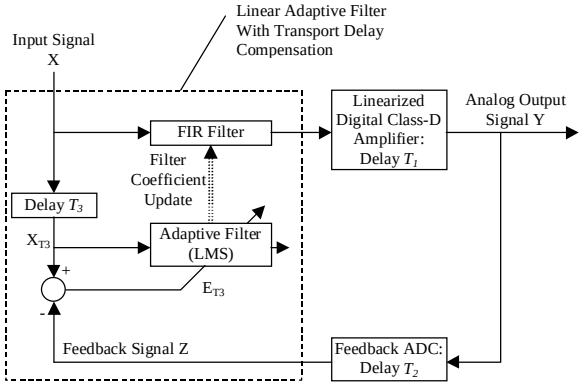


Figure 6.2 Adaptive Filter with Transport Delay Compensation

The system of Figure 6.2 can be modified further to eliminate the additional FIR filter. The optimized system is shown in Figure 6.3. The modified adaptive filter updates its weights now using the delayed version of the input signal (X_{T3}).

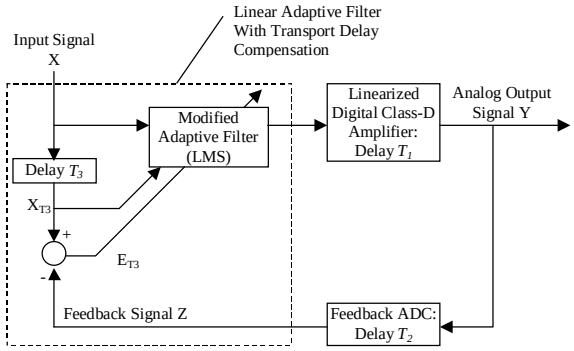


Figure 6.3 Optimized Adaptive Filter with Transport Delay Compensation

A detailed description of linear adaptive filters can be found in [10]. The linear adaptive filter can be used with any system-inherent delay, but it would only compensate slow changes and, importantly, linear changes in the system. However, this would be sufficient to compensate for variable load effects and guarantee a maximally flat magnitude and phase response of the amplifier, which is very important for HIFI stereophony . As many analog Class-D amplifiers have feedback structures that do not encompass the output filter for stability reasons [4], the linear adaptive filter would be equally useful in those systems.

7 CONLUSIONS

This paper describes the simulation and implementation of a digital Class-D audio amplifier. Three PWM linearization techniques have been evaluated using a MATLAB SIMULINK simulation. Two methods were implemented in a laboratory prototype amplifier. Both methods were shown to work. The DSP-based prototype amplifier introduced in this paper allows easy real-time verification of simulated systems and performance evaluation. A single processor solution was achieved with the powerful TMS320C6701 signal processor. Alternative DSP algorithms can be easily implemented without having to change the hardware of the laboratory prototype amplifier.

As a new approach to the feedback problem of digital Class-D amplifiers this paper proposed the application of a linear adaptive filter.

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